First Call For Papers

2025 IEEE 16th International Conference on ASIC

Oct. 21-24, 2025, Crowne Plaza Kunming City Centre

Kunming, China

Sponsored by	*IEEE Beijing Section*
Co-Sponsored by	*Fudan University*
	Yunnan University
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2025 IEEE 16th International Conference on ASIC (ASICON 2025) will be held in Kunming, China, during Oct. 21-24, 2025. The conference is intended to provide an international forum for Integrated circuit designers, system integrators, IC manufacturers, process and device engineers, and CAD/CAE tool developers to present their latest progress, development and research results in their respective fields. The four-day event features keynote speeches, invited talks, regular paper presentations and tutorials, delivered by leading experts in the respective fields, on state-of-the-art Integrated circuits, design methodologies, devices, processes and manufacturing technologies. The Excellent Student Paper Award & Outstanding Young Scholar Paper Award will be announced at the conference. Additionally, an exhibition on EDA tools, foundry technologies, IC processing/testing facilities, and novel ASIC products will be held during the conference.

The Scope of the Conference

Papers are solicited in, but not limited to, the following:

I. Integrated Circuits and Design Techniques

[1] **Analog IC**
- Amplifiers,
- Data converters (ADCs and DACs)
- Power management ICs and Energy Harvesting
- Clock generator

[2] **Digital IC**
- Low power technique
- CPU, MCU, GPU, Embedded processors and DSP
- Chaos/neural/fuzzy-logic circuits
- Programmable devices (PLD, EPLD, HDPLD, FPGA, etc)
- NOC

[3] **Wireless, Wireline telecommunication and Optic Communication IC**
- RF block circuits (LNA, Mixer, PA, Integrated Antenna and Switches),
- RF Transceiver (Transmitter, receiver, PLL in RF transceiver), RFID
- millimeter-wave circuits
- Seders
- THz circuits,
- Laser Driver, TIA, CDR

[4] **Memory**
- DRAM & SRAM
- Flash memory
- Ferroelectric memory
- Phase change memory, RRAM, MRAM
- Novel memory

[5] **Sensor, Image Processing and Bio-medical IC**
- Sensor circuits
- Graph theory and computing
- Biomedical circuits and systems
- Wearable systems

[6] **FPGA and DSP**
- FPGA architecture and circuits
- Reconfigurable technique,
- DSP architecture and circuits
- FPGA and DSP application

[7] **Special application IC**
- Automobile IC,
- Anti-Radiation IC
- Ultra-High Voltage Circuits

[8] **Design for Testing**
- Digital/analog/mix-signal testing
- Design for testability and reliability

- Test vector compression and silicon debug and diagnosis
- Variation-aware design
- Static and dynamic defect and fault recoverability

II. Artificial Intelligence Chip

[9] **Graphics Processing Units**

- Machine learning
- Video and graphics processing
- GPU virtualization
- Scientific computing and simulation

[10] **FPGAs for AI**

- Edge AI
- Embedded AI
- AI workloads acceleration

[11] **Special AI chips**

- Brain-like chip
- Neural network chip
- Tensor Processing Unit

III. CAD Techniques

[12] **Circuits Simulation, Synthesis, Verification and Physical Design**

- Analog circuits modeling and simulation
- Logic synthesis, simulation and formal verification
- Partitioning, placement and floor planning
- Routing and detailed physical design

[13] **CAD for System, Design for Manufacturing and Testing**

- Embedded systems
- Mixed technology/domain, reliable and alternative systems
- Design for manufacturability and testing

IV. New Techniques, New Processing, New Devices and Their Applications

[14] **MEMS Techniques**

- Piezoelectric and MEMS application
- Pyroelectric/IR/optical application
- Sensors, chemical and bio-chips

[15] **Nano-electronics and Giga-scale Systems:** Nano devices and NEMS

[16] **New Devices:** Hetero-junction Devices, Fin FET, CNT MTJ Devices, 3-D Integration, etc.

[17] **New Processing:** Advanced Interconnection Technology, High-K/Metal Gate Technology and Other VLSL New Processing

[18] **Processing Modeling & Simulation**

V. Other VLSI Design and Device Related Topics

[19] **Other Devices Related Topics**

[20] **Other VLSI Design Related Topics**

Papers Submission

Prospective authors are requested to submit full-length papers in English of no more than four pages using the proceedings format, double columned, 10pt fonts including figures, tables and references. For further information on the paper format, please refer to "template". The papers are submitted in their final form, if accepted, will be published as submitted. All submissions must be made at the conference website. Authors who want to compete for the Excellent Student or Outstanding Young Scholar Paper Award should apply at the conference website. Detailed instructions for paper preparation and submission can be found at conference website. **Tutorial proposals are also invited.**

Contact persons: **Prof. Huihua Yu** (Conference Issue) Email: asicon_org@fudan.edu.cn

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For further information please visit conference web site:

http://www.asicon.org

Deadline of papers submittal is June 30, 2025

Paper acceptance/rejection will be informed by Aug. 15, 2025