

**2019 IEEE 13th International Conference on ASIC
(ASICON)**



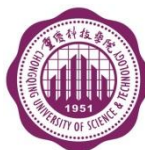
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ASICON 2019

ADVANCE PROGRAM

Oct. 29 - Nov. 1, 2019

Hotel Hilton, Chongqing, China





**2019 IEEE 13th International
Conference on ASIC
(ASICON)**

ASICON 2019

Oct. 29 - Nov. 1, 2019
Hotel Hilton, Chongqing, China

Sponsored by

IEEE Beijing Section
Fudan University

Supported by

Chongqing University
Chongqing University of Science and Technology
IEEE CASS
IEEE SSCS Shanghai Chapter
IET Shanghai Network
Chinese Institute of Electronics (CIE)

Organized by

Fudan University

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Welcome to ASICON 2019

On behalf of the Conference, it is our great pleasure and honor to express our warm welcome to all ASICON 2019 attendees. Thank you very much for your participation.

ASICON 2019 is the 13th event of this conference series that began in 1994. The Conference will be held from October 29 to Nov.1, 2019 at Hilton Hotel, Chongqing, China. Chongqing is one of the four municipalities directly under the central government and an important city in southwest China. We sincerely hope that you will have a rewarding and good time in Chongqing.

While “ASIC” has had a narrow meaning, the Conference has adopted **A**dvanced **S**emiconductor **I**ntegrated **C**ircuits as the meaning of ASIC in ASICON. This is in recognition of the fact that ASICON covers broad technical fields of integrated circuits. The conference provides an international forum for VLSI circuit designers, ASIC users, System Integrators, IC manufacturers, devices engineers and CAD/CAE tool developers to present the latest progresses, development and research results in their respective fields. The Conference also serves as a platform for academic and industry attendees to network and exchange information.

ASICON 2019 has invited four international experts to give tutorials on the first day of the conference. In addition, we have invited 8 world renowned academic and industry leaders to give keynote speeches during the plenary sessions from Oct.30-Nov.1.

ASICON has had a very significant impact on industry and academia. We look forward to continuing this tradition with you at this year’s conference.

General Co-Chairs of ASICON 2019

Jan Van der Spiegel
Ting-Ao Tang
Yong Lian
Zhiliang Hong
Xiaoping Zeng

Oct. 30, 2019

Conference Committee

General Co-Chairs

Name	Affiliation	Country/Area
Jan Van der Spiegel	University of Pennsylvania	USA
Ting-Ao Tang	Fudan University	China
Yong Lian	York University	Canada
Zhiliang Hong	Fudan University	China
Xiaoping Zeng	Chongqing University	China

Advisory Committee Co-Chairs

Chenming Hu	UC Berkeley	USA
Omar Wing	Columbia University	USA
Richard.M.M. Chen	IEEE HK Section	Hongkong, China
Hiroshi Iwai	Tokyo Institute of Technology	Japan
Satoshi Goto	Waseda University	Japan
Qianling Zhang	Fudan University	China

Program Committee Co-Chairs

Yinyin Lin	Fudan University	China
Bin Zhao	Fairchild	USA
Hidetoshi Onodera	Kyoto University	Japan
Jyi-Tsong Lin	National Sun Yat-sen University	Taiwan, ROC
Francois Rivet	University of Bordeaux	France
Yi Zhao	Zhejiang University	China

Organizing Committee Co-Chairs

Mengqi Zhou	IEEE Beijing Section	China
Huihua Yu	Fudan University	China
Min Liu	Chongqing University	China

Industry Liaison

Peng Hu	CICMAG Com	China
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Secretary-General

Fan Ye	Fudan University	China
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Technical Program Committee Members of ASICON 2019

Analog and RF Circuits Subcommittee

Chen, Weizen	National Chiao Tung University	Taiwan, ROC
Huang, Mo	South China University of Technology	China
Lee, Tai-Cheng	National Taiwan University	Taiwan, ROC
Zhang, Feng	institute of microelectronics, CAS	China
Kobayashi, Haruo	Gunma University	Japan
Simon, Ang	University of Arkansas	USA
Song, Fei	Ubilinx technology, Inc	USA
Wu, Nanjian	Institute of Semiconductor, CAS	China
Xiang, Yi	Chongqing University of Science & Technology	China

Digital Circuits and SOC Subcommittee

Zhang, Wenjun	Intel	USA
Qu, Gang	University of Maryland	USA
John, Deepu	University College Dublin	Ireland
Wang, Pengjun	Wenzhou University	China
Liu, Dongsheng	Huazhong University of Science and Technology	China
Wang, Shaoyun	NextInput, Inc.	USA

Wang, Chua-Chin	National Sun Yat-Sen University	Taiwan, ROC
Sobelman, Gerald	University of Minnesota	USA
Gong, Na	University of South Alabama	USA
Jou, Shyh-Jye	National Chiao Tung University	Taiwan, ROC
Sang, Tzu-Hsien	National Chiao Tung University	Taiwan, ROC
Liu, Liang	Lund University	Sweden
Min, Kyeong-Sik	Kookmin University	Korea
Ikeda, Makoto	University of Tokyo	Japan
Yu, Zhiyi	Sun Yat-sen University	China
Wen, Xiaoqing	Kyushu Institute of Technology	Japan
Zhang, Chuan	Southeast University	China
Chen, Guorong	Chongqing University of Science & Technology	China

CAD Techniques Subcommittee

Sheldon, Tan	University of California, Riverside	USA
Qu, Gang	University of Maryland	USA
Yu, Bei	Chinese University of Hong Kong	China
Jerraya, Ahmed	CEA Tech	France
Wang, Xingang	Skyworks Solutions, Inc.	USA
Wen, Xiaoqing	Kyushu Institute of Technology	Japan
Wu, Ying	Chongqing University of Science & Technology	China

Process and Devices Subcommittee

Chang-Liao, Kuei-Shu	National Tsing Hua University	Taiwan, ROC
LAI, Chao-Sung	Chang Gung University	Taiwan, ROC
Kobayashi, Masaharu	The University of Tokyo	Japan
Chan, Mansun	Hong Kong University of Science and Technology	Hong Kong, China
Chen, Kuan-Neng	National Chiao Tung University	Taiwan, ROC
Jerraya, Ahmed	CEA Tech	France
Lee, Ching-Ting	National Cheng Kung University/Yuan	Taiwan, ROC

	Ze University	
Li, Pei-Wen	National Chiao Tung University	Taiwan, ROC
Zhao, Weisheng	Beihang University	China
Simon, Ang	University of Arkansas	USA
Ng, Wai Tung	University of Toronto	Canada
Simoen, Eddy	IMEC	Belgium
Endo, Kazuhiko	Advanced Industrial Science and Technology (AIST)	Japan
Zhang, Jian Fu	Liverpool John Moores University	UK
Zhang, Weidong	Liverpool John Moores University	UK
Xie, Ya-Hong	University of California, Los Angeles	USA
Yi, Jun	Chongqing University of Science & Technology	China

General Information

● Conference Language

The official language is English. No simultaneous translation is available.

● Conference Schedule

Date	Time	Event
Oct. 29 Tue.	AM & PM	Tutorial Session & Registration
Oct. 30 Wed.	AM	Opening & Keynote Session
		Keynote Session (K-1,K-2)
	PM	Parallel Sessions
		Parallel Sessions
		IEEE CASS YP Session Poster Session (1)
	Evening	Reception
Oct. 31 Thur.	AM	Keynote Session (K-3)
		Parallel Sessions
	PM	Parallel Sessions
		Parallel Sessions Poster Session (2)
Nov. 1 Fri.	AM	Keynote Session (K-4)
		Parallel Sessions
	PM	Parallel Sessions
		Parallel Sessions
	Evening	Banquet

● Conference Site

The conference will be held in **Hotel Hilton Chongqing*******

Tel: +86-23-89039999

Add: No.139 Zhong Shan San Road, Yuzhong District, Chongqing, China

Website: <http://www.hilton.com.cn/zh-cn/hotel/Chongqing/hilton-Chongqing-CKGHIHI/index.html>

● Conference Registration

Payment by Credit Card, Bank Transfer, or Check

1. **Participant:** **Accepted Paper ID Number**(if available): _____

☐ Mr. ☐ Ms. First Name: _____ Last Name: _____

Affiliation (Univ./Company): _____

Address: _____

Phone: _____ Mobile: _____ Email: _____

2. Registration Fee

Classification	Before Sep.15, 2019	After Sep.15, 2019	Amount
IEEE or IET member★	<input type="checkbox"/> 3500 CNY	<input type="checkbox"/> 3800 CNY	
Non-member	<input type="checkbox"/> 3800 CNY	<input type="checkbox"/> 4100 CNY	
Student	<input type="checkbox"/> 2500 CNY	<input type="checkbox"/> 2800 CNY	
Extra banquet ticket	<input type="checkbox"/> 300 CNY		
Extra pages	<input type="checkbox"/> 400 CNY / page		
Tutorial	<input type="checkbox"/> T-1 & T-2 & T-3 & T-4 200 CNY		
Hardcopy	<input type="checkbox"/> Need hardcopy Proceedings 500 CNY <input type="checkbox"/> Don't need hardcopy Proceedings		
TotalAmount	CNY		

(★IEEE or IETMember)★ Member Number: _____

The registration fee covers:

- Admission to all the sessions;
- Three days' meals (Oct.30-Nov.1, 2019) including the reception (Evening of Oct.30) and the banquet (Evening of Nov.1); Coffee Breaks;
- A conference kit (with a conference bag, a program brochure, and a USB with E-Proceedings).

(The tutorial fee covers the lunch on Oct.29 and tutorial materials. Please visit the conference website for details of the tutorials.)

3. Payment Methods

1) <input type="checkbox"/> Credit Card Date of Payment _____	Please Click Here for Credit Card Payment	_____ CNY
2) <input type="checkbox"/> Bank Transfer Remit date _____ Note: If it is not possible for you to transfer CNY, please transfer USD based on the	Sender's Name _____ Account Name: <u>GUILIN COMFORT INTERNATIONAL TRAVEL SERVICE CO., LTD.</u> Account Number: <u>453801000018010145542</u> Bank Name: <u>BANK OF COMMUNICATIONS, GUILIN BRANCH</u> Bank address: <u>No. 8 NANHUAN ROAD, GUILIN,</u>	_____ CNY

USD/CNY exchange rate of the day of transfer.	<u>GUANGXI, CHINA</u> Swift Code: <u>COMMCNSHGLN</u> CNAPS NUMBER: <u>301617000010</u> Attn: ASICON 2019	
3) <input type="checkbox"/> Bank Draft/Check Remit date_____	I have enclosed herewith a bank draft/check made payable to Fudan University and sent to Jieting Sheng	_____ CNY

Please send the Registration Form and Payment Receipt to Jieting Sheng by Email

Email: jtsheng@fudan.edu.cn

Mailing address: School of Microelectronics, Fudan University,
220 Handan Road, Shanghai, 200433, China

● Registration Desk

The conference registration desk will be located at Chongqing Hilton Hotel. The conference registration will be open on Oct. 29 (8: 00~20: 00), Oct. 30~Nov. 1 (8: 00~17: 45). And the registration desk will keep available at the same site throughout the whole conference.

● Transportation

How to get to the Hilton Chongqing:

- It takes about 35 minutes from Chongqing Jiangbei International Airport to Hotel by car. Taxi is recommended.
- Chongqing North Railway Station: Taxi takes about 20 minutes to hotel
- Chongqing Railway Station: Walk about 10 minutes to hotel

More details about the conference hotel booking, please visit

<https://www.discoverchinatours.com/chongqing-asicon-2019-hotel.html>

● Weather

The average temperature during conference time in Chongqing is around 14°C~19°C.

● Visa

All the foreign travelers to China must have a valid visa. Visas may be obtained from the Chinese Embassy or Consulate in most major cities around the world. A conference attendee will be mailed an official invitation letter for visa application after he or she fills and returns the Visa Application Form (<http://www.asicon.org>) to asicon_org@fudan.edu.cn timely.

● Awards

Excellent Student Paper Awards will be announced at the banquet on Nov. 1. To be qualified for the Excellent Student Paper Award, the paper must be presented by the student himself or herself (1st author). The Technical Program Committee and Organizing Committee will choose through public appraisal some excellent student papers from the candidates.

Paper Presentation Information

The ASICON2019 will have oral and poster sessions. All the papers included in the conference program should be presented in English by one of the authors at the arranged sessions.

● Oral Presentation

Presentation time:

Invited paper (20~30 minutes): 15~25 min talk + 5 min Q/A

Regular paper (10~15 minutes): 10~12 min talk + 2~3 min Q/A

Computer and digital projector will be provided in each meeting room.

● Poster Presentation

Poster size: 120 cm (high) × 100 cm (wide)

Poster Session 1:

Setup time: 8: 30-17: 30 on Oct. 30

Presentation time: 17: 45-18: 45 on Oct. 30 (on the spot)

Poster Session 2:

Setup time: 8: 30-17: 30 on Oct. 31

Presentation time: 17: 45-18: 45 on Oct. 31 (on the spot)

Thumb pins, adhesive tapes, and scissors will be provided at the registration desk. The poster should be taken off by 21: 30 by the author if he or she would like to keep it. After that time, it will be removed and be regarded as being discarded by the authors.

● Coffee Break

Complementary coffee/tea will be served in each morning/afternoon session. The break will take place in general at 10: 00-10: 15 during morning sessions and 15: 30-15: 45 during afternoon sessions. Due to time schedule of different sessions, the actual break time may have slight variation. Coffee/tea will be served in about half-hour duration.

● Meeting Room Location

Meeting Room	Location
Grand Ball Room	Hotel Hilton 3 rd Floor
Happiness Room	Hotel Hilton 3 rd Floor
Fortune Room	Hotel Hilton 3 rd Floor
Xi'An + Dalian Room	Hotel Hilton 4 th Floor
Wuhan + Nanjing Room	Hotel Hilton 4 th Floor

Tutorial Session

Tuesday, October 29, 9: 00 – 17: 15

Tuesday, October 29, 9: 00 – 12: 15

Meeting Room: “Xi’an+Dalian”

Tutorial Session T-1 & T-2

Hilton Hotel 4th Floor

Session Chair: Fan Ye

T-1 Negative Capacitor Field Effect Transistors (NC-FET) (9: 00-10: 30)

Prof. Muhammad A. Alam, University of Purdue, USA

T-2 Single-Bit Delta-Sigma Modulation Techniques for Robust Communication Systems (10: 45-12: 15)

Prof. Woogeun Rhee, Tsinghua University, China

Tuesday, October 29, 14: 00 – 17: 15

Meeting Room: “Xi’an+Dalian”

Tutorial Session T-3 & T-4

Hilton Hotel 4th Floor

Session Chair: Zhiliang Hong

T-3 Radiation Hardening by Design of Digital Circuits (14:00-15: 30)

Prof. Kazutoshi Kobayashi, Kyoto Institute of Technology, Japan

T-4 Low Power Smart Sensor Node Processor design (15: 45-17: 15)

Prof. Jun Zhou, University of Electronic Science and Technology of China, China

Technical Session

Wednesday

Wednesday, October 30, 9: 00 –10: 30

Wednesday, October 30, 9: 00 –10: 30

Grand Ball Room

Opening & Keynote Session K1

Hotel Hilton 3rd Floor

Session Chair: Jan Van der Spiegel

K1-1 Extending Moore's Law Scaling Through Integrated Materials Systems

(9: 00-9: 45)

Dr. Sanjay Natarajan, VP, Applied Materials, USA

K1-2 Implantable Brain Microdevices for the Treatment of Neurodegenerative Diseases

(9: 45-10: 30)

Prof. Mohamad Sawan, Polytechnique Montréal, Canada, Westlake University, China

Wednesday, October 30, 10: 45– 12: 15

Wednesday, October 30, 10: 45–12: 15

Grand Ball Room

Keynote Session K2

Hotel Hilton 3rd Floor

Session Chair: Rechar. M. M. Chen

K2-1 Systematic Design of Low-power Analog and RF CMOS Circuits *(10: 45-11: 30)*

Prof. Christian Enz, EPFL, Switzerland

K2-2 Video Coding for Machines -Standard and ASIC *(11: 30-12: 15)*

Dr. Lin Yang, Chief Scientist of Gyrfalcon Technology, Inc, USA

Wednesday, October 30, 13: 30 – 15: 30

Wednesday, October 30, 13: 30 – 15: 30	Xi'an + Dalian Room
Session A1 : Digital Unit & Module	Hotel Hilton 4 th Floor
Session Chair : Chua-Chin Wang	

	Title
A1-1	0703: Non-linear function evaluation reusing matrix-vector multipliers (Invited Paper)
13: 30	Ce Guo, Wayne Luk, Wenguang Xu (<i>Imperial College London; Huawei Technologies</i>)
A1-2	0813: A Polymorphic Circuit Interoperability Framework (Invited Paper)
13: 52	Timothy Dunlap, Gang Qu, Jingmei Lai (<i>University of Maryland, USA; State Key Library of ASIC and System, Fudan University</i>)
A1-3	0660: Design of Crosstalk NAND Gate Circuit Based on Interconnect Coupling Capacitance
14: 14	Zhiwei Zhao, Yuejun Zhang, Pengjun Wang, Huihong Zhang, Weishan Zhang (<i>Faculty of Electrical Engineering and Computer Science, Ningbo University</i>)
A1-4	0394: Soft-Error Tolerance Depending on Supply Voltage by Heavy Ions on Radiation-Hardened Flip Flops in a 65 nm Bulk Process
14: 25	Yuto Tsukita, Mitsunori Ebara, Jun Furuta, and Kazutoshi Kobayashi (<i>Kyoto Institute of Technology, Japan</i>)
A1-5	0630: Novel High-Performance and Cost Effective Soft Error Hardened Flip-Flop Design for Nanoscale CMOS Technology
14: 36	Hong-Chen Li, Li-Yi Xiao, Jie Li, He Liu (<i>Microelectronic center, Harbin Institute of Technology</i>)
A1-6	0509: A Radiation Hardened Clock Inverter Cell with High Reliability for Mitigating SET in Clock Network
14: 47	Jie Li, Liyi Xiao, Hongchen Li, Lulu Liao, Chenxu Wang (<i>Microelectronics Center, Harbin Institute of Technology</i>)
A1-7	0655: A High-speed Dynamic Domino Full Adder Based on DICG Positive Feedback
14: 58	Xiaotian Zhang, Pengjun Wang, Yunfei Yu, Yuejun Zhang, Shunxin Ye (<i>Faculty of Electrical Engineering and Computer Science, Ningbo University</i>)
A1-8	0661: Area Optimization of MPRM Circuits Using Approximate Computing
15: 09	QiuHong Ying, LunYao Wang, ZhuFei Chu, YinShui Xia (<i>Faculty of Electrical Engineering & Computer Science, Ningbo University</i>)

A1-9	0341: Power optimization for FPRM logic using approximate computing technique
15: 20	Yichen Wang, Lunyao Wang (<i>Faculty of Electrical Engineering & Computer Science, Ningbo University</i>)

Wednesday, October 30, 13: 30 – 15: 30	Wuhan + Nanjing Room
Session B1 : Efficient AI Hardware	Hotel Hilton 4 th Floor
Session Chair : Kyeong-Sik Min	

	Title
B1-1	0773: Genetic Architecture Search for Binarized Neural Networks (Invited Paper)
13: 30	Yangyang Chang, Gerald E. Sobelman, Xiaofang Zhou (<i>Dept. of Electrical and Computer Engineering, University of Minnesota; State Key Lab of ASIC and Systems, Fudan University</i>)
B1-2	0565: Ultra-Low-Power Intelligent Acoustic Sensing using Cochlea-Inspired Feature Extraction and DNN Classification (Invited Paper)
13: 54	Minhao Yang, Shih-Chii Liu, Mingoo Seok, Christian Enz (<i>Institute of Microengineering, EPFL; Institute of Neuroinformatics, UZH/ETH Zurich; Department of Electrical Engineering, Columbia University...</i>)
B1-3	0501: BNReLU: Combine Batch Normalization and Rectified Linear Unit to Reduce Hardware Overhead
14: 18	Jiexian Ge, Xiaoxin Cui, Kanglin Xiao, Chenglong Zou, YiHsiang Chen, Rongshan Wei (<i>College of Physics and Information Engineering, Fuzhou University; Key Laboratory of Microelectronics Devices and Circuits, Institute of Microelectronics, Peking University</i>)
B1-4	0428: An Efficient Accelerator for Sparse Convolutional Neural Networks
14: 30	Weijie You, Chang Wu (<i>State-Key Lab of ASIC and System, Fudan University</i>)
B1-5	0739: An Energy-Efficient Systolic Pipeline Architecture for Binary Convolutional Neural Network
14:42	Baicheng Liu, Song Chen, Yi Kang, and Feng Wu (<i>School of Microelectronics, University of Science and Technology of China</i>)
B1-6	0336: Energy-Efficient Hardware Architecture of Embedded Machine Learning
14: 54	Osman Elgawi (<i>University of California, Los Angeles</i>)
B1-7	0707: A Grain-Adaptive Computing Structure for FPGA CNN Acceleration
15: 06	Xinyuan Qu, Zhihong Huang, Ning Mao, Yu Xu, Gang Cai, Zhen Fang (<i>State Key Laboratory of Transducer Technology, Institute of Electronics Chinese Academy of Sciences; School of Electronic, Electrical, and Communication Engineering, University of Chinese Academy of Sciences</i>)

B1-8	0784: An Optimized Face Recognition for Edge Computing
15: 18	Luchang Ding, Yuan Xie, Jiarui Zhou, Gengsheng Chen (<i>State-Key Lab of ASIC and System, Fudan University</i>)

Wednesday, October 30, 13: 30 – 15: 30	Happiness Room Hotel Hilton 3 rd Floor
Session C1 : Security Technology	
Session Chair : Dongshen Liu	

	Title
C1-1	0794: On-Chip Protection of Cryptographic ICs Against Physical Side Channel Attacks (Invited Paper)
13: 30	Makoto Nagata (<i>Graduate School of Science, Technology and Innovation, Kobe University</i>)
C1-2	0775: Hardware Acceleration of Functional Cryptography (Invited Paper, abstract only)
14:00	Makoto Ikeda (<i>VLSI Design and Education Center, the University of Tokyo</i>)
C1-3	0684: Design of Asynchronous High Throughput SHA-256 Hardware Accelerator in 40nm CMOS
14: 30	Junshang Li, Zishang He, Yajie Qin (<i>State Key Laboratory of ASIC & System, Fudan University</i>)
C1-4	0709: Method for improving energy efficiency of elliptic curve cryptography algorithm on reconfigurable symmetric cipher processor
14: 45	Zhao Tuo, Tao Chen, Wei Li, Danyang Yang (<i>Department of microelectronics, institute of information science and technology</i>)
C1-5	0737: Security Analysis and Modeling Attacks on Duty Cycle Multiplexer PUF
15: 00	Yunhao Xu, Yingjie Lao, Weiqiang Liu, and Chuan Zhang (<i>Lab of Efficient Architectures for Digital-communication and Signal-processing; National Mobile Communications Research Laboratory, Southeast University...</i>)
C1-6	0468: SVM Based Network Intrusion Detection for the UNSW-NB15 Dataset
15: 15	Dishan Jing and Hai-Bao Chen (<i>Department of Micro and Nano Electronics, Shanghai Jiaotong University</i>)

Wedsday, October 30, 13: 30 – 15: 30	Fortune Room Hotel Hilton 3 rd Floor
Session D1 : Power Device	
Session Chair : Mengyuan Hua	

	Title
D1-1	0514: High Reliability GaN FET Gate Drivers for Next-generation Power Electronics Technology (Invited Paper)

13: 30	Xin Ming, Zhi-wen Zhang, Zi-wei Fan, Yao Qin, Yuan-yuan Liu, Bo Zhang (<i>State key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China</i>)
D1-2	0774: An Enhancement-mode GaN FEG-HEMT Device for Power Switching Applications (Invited Paper, abstract only)
14: 00	Edward Yi Chang (<i>National Chiao Tung University</i>)
D1-3	0786: Smart Gate Driver ICs for GaN Power Transistors (Invited Paper)
14: 30	Wei Jia Zhang, Jingshu Yu, and Wai Tung Ng (<i>The Edward S. Rogers Sr. Department of Electrical and Computer Engineering University of Toronto</i>)
D1-4	0702: Switching of 3300V Scaled IGBT by 5V Gate Drive (Invited Paper)
15: 00	T. Hiramoto, T. Saraya, K. Itou, T. Takakura, M. Fukui, S. Suzuki, K. Takeuchi, M. Tsukuda, Y. Numasawa, K. Satoh, T. Matsudai, W. Saito, K. Kakushima, T. Hoshii, K. Furukawa, M. Watanabe, N. Shigyo, H. Wakabayashi, K. Tsutsui, H. Iwai, A. Ogura, S. Nishizawa, I. Omura, H. Ohashi (<i>The University of Tokyo...</i>)

Wednesday, October 30, 15: 45-17: 45

Wednesday, October 30, 15: 45-17: 45

Xi'An + Dalian Room

Session A2 : Signal Processing

Hotel Hilton 4th Floor

Session Chair : Ngai Wong

	Title
A2-1	0649: Analog / Mixed-Signal / RF Circuits for Complex Signal Processing (Invited Paper)
15: 45	Haruo Kobayashi, Nene Kushita, Minh Tri Tran, Koji Asami, Hao San, Anna Kuwana, Akemi Hatta (<i>Division of Electronics and Informatics, Gunma University; Tokyo City University</i>)
A2-2	0768: LiDAR Point Cloud Generation and Defogging for Vehicular Applications (Invited Paper, abstract only)
16: 15	Tzu-Hsien Sang, Tsai Song-You, Chia-Ming Tsai (<i>Institute of Electronics Engineering, NCTU</i>)
A2-3	0540: Analysis and Evaluation Method of RC Polyphase Filter
16: 45	Koji Asami, Nene Kushita, Akemi Hatta, Minh Tri Tran, Yoshiro Tamura, Anna Kuwana, Haruo Kobayashi (<i>Advantest Laboratories Ltd, Japan; Division of Electronics and Informatics, Gunma University</i>)
A2-4	0353: Flat Pass-Band Method with Two RC Band-Stop Filters for 4-Stage Passive RC Polyphase Filter in Low-IF Receiver Systems

16: 57	Minh Tri Tran, Nene Kushita, Anna Kuwana, and Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University, Japan</i>)
A2-5	0530: Frequency Estimation Sampling Circuit Using Analog Hilbert Filter and Residue Number System
17: 09	Yudai Abe, Shogo Katayama, Congbing Li, Anna Kuwana, Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University, Japan</i>)
A2-6	0473: An Adder-Segmentation-based FIR for High Speed Signal Processing
17: 21	Jinghao Ye, Masao Yanagisawa and Youhua Shi (<i>Graduate School of Fundamental Science and Engineering, Waseda University, Tokyo</i>)
A2-7	0459: An Optimal Designed Compensator for PSR Flyback Converters Based on Genetic Algorithm
17: 33	Tianyuan Tang, Ping Luo, Chengda Deng, Qiang Wang, Liao Zhang, Bo Zhang (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China,</i>)

Wednesday, October 30, 15: 45-17: 45	Wuhan + Nanjing Room
Session B2 : Computing-in/near-Memory I	Hotel Hilton 4 th Floor
Session Chair : Minhao Yang	

	Title
B2-1	0572: Defect-Tolerant and Energy-Efficient Training of Multi-Valued and Binary Memristor Crossbars for Near-Sensor Cognitive Computing (Invited Paper)
15: 45	Khoa Van Pham, Tien Van Nguyen, and Kyeong-Sik Min (<i>School of Electrical Engineering, Kookmin University, Korea</i>)
B2-2	0493: Circuit Design Challenges in Computing-in-Memory for AI Edge Devices (Invited Paper)
16: 15	Xin Si, Cheng-Xin Xue, Jian-Wei Su, Zhixiao Zhang, Sih-Han Li, Shyh-Shyuan Sheu, Heng-Yuan Lee, Ping-Cheng Chen, Huaqiang Wu, He Qian, and Meng-Fan Chang (<i>National Tsing Hua University; University of Electronic Science and Technology of China</i>)
B2-3	0699: CoDRAM: A Novel Near Memory Computing Framework with Computational DRAM
16: 45	Yu Ma, Linfeng Zheng and Pingqiang Zhou (<i>School of Information Science and Technology, ShanghaiTech University</i>)
B2-4	0535: FNSim: A Device-Circuit-Algorithm Codesigned Simulator for Flash based Neural Network
17: 15	Min Zhang, Peng Huang, Yizhou Zhang, Yachen Xiang, Runze Han, Lifeng Liu, Xiaoyan Liu, Jinfeng Kang (<i>Institute of Microelectronics, Peking University</i>)

Wednesday, October 30, 15: 45-17: 45	Happiness Room
Session C2 : ADC Circuit	Hotel Hilton 3 rd Floor
Session Chair : Yongzheng Chen	

	Title
C2-1	0781: Circuit Design Challenges of ADC for the Application in Multiple Physiological Parameters Detection System (Invited Paper)
15: 45	Ye Yuan, Song Ma, and Yuhua Cheng (<i>Shanghai Research Institute of Microelectronics, Peking University; School of EECS, Peking University</i>)
C2-2	0444: Sampling Rate Enhancement for SAR-ADCs Using Adaptive Reset Approach for FOG Systems (Invited Paper)
16: 10	Chun-Ting Chen, Tsung-Yi Tsai, Yi-Jen Chiu, and Chua-Chin Wang (<i>Department of Electrical Engineering National Sun Yat-Sen University</i>)
C2-3	0328: A SAR-Assisted Continuous-Time Incremental $\Sigma\Delta$ ADC With First-Order Noise Coupling (Invited Paper)
16: 35	Yu-Lun Hsieh and Tai-Cheng Lee (<i>Graduate Institute of Electronics Engineering, National Taiwan University</i>)
C2-4	0384: High-Resolution Low-Sampling-Rate $\Delta\Sigma$ ADC Linearity Short-Time Testing Algorithm
17: 00	Jiang-Lin Wei, Nene Kushita, Takahiro Arai, Lei Sha, Anna Kuwana, Haruo Kobayashi, Takayuki Nakatani, Kazumi Hatayama, Keno Sato, Takashi Ishida, Toshiyuki Okamoto, Tamotsu Ichikawa (<i>Division of Electronics and Informatics, Faculty of Science and Technology, Gunma University; ROHM Semiconductor Co., Ltd.</i>)
C2-5	0479: Multibit Sturdy MASH $\Delta\Sigma$ Modulator with Error-shaped Segmented DACs for Wideband Low-power Applications
17: 15	Liang Qi, Sai-Weng Sin, Rui Paulo Martins (<i>State-Key Laboratory of Analog and Mixed-Signal VLSI/Institute of Microelectronics-IME, Also with Department of ECE/Faculty of Science and Technology, University of Macau</i>)
C2-6	0746: A 10b 250MS/s SAR ADC with Speed-Enhanced SAR Logic and Free Time More Than a Half of Sampling Period
17: 30	Shumin Zhang, Yuefeng Cao, Fan Ye and Junyan Ren (<i>State Key Laboratory of ASIC and System, Fudan University</i>)

Wednesday, October 30, 15: 45-17: 45	Fortune Room
Session D2 : Device Simulation & Integration I	Hotel Hilton 3 rd Floor
Session Chair : Toshiro Hiramoto	

	Title
D2-1	0364: Comprehensive Understanding of Negative Capacitance FET From the Perspective of Transient Ferroelectric Model (Invited Paper)
15: 45	Masaharu Kobayashi, Chengji Jin, Toshiro Hiramoto (<i>VLSI Design and Education Center, The University of Tokyo; Institute of Industrial Science, The University of Tokyo</i>)
D2-2	0317: Impact of Device Architecture and Gate Stack Processing on the Low-Frequency Noise of Silicon Nanowire Transistors (Invited Paper)
16: 15	Eddy Simoen, Alberto Vinicius Oliveira, Anabela Veloso, Adrian Vaisman Chasin, Romain Ritzenthaler, Hans Mertens, Naoto Horiguchi, Cor Claeys (<i>Imec, Belgium; UTFPR, Campus Toledo, Brazil; EE Depart. KU Leuven, Belgium</i>)
D2-3	0763: Performance Investigation of Uniaxially Tensile Stressed Ge n-FinFETs Formed on Biaxially Strained GeOI Substrates And Its Impact On Ge CMOS Inverters
16: 45	Ran Cheng, Ming Tian, Changfeng Wang, Zhimei Cai, Jie Zhang, Yan-Yan Zhang, and Yi Zhao (<i>College of Information Science and Electronic Engineering, Zhejiang University; Shanghai Huali Microelectronics Corporation</i>)
D2-4	0690: Variation Analysis of Interconnect Capacitance and Process Corner in Advanced CMOS Process with Double Patterning Technology
17: 00	Zhimei Cai, Zhiyong Han, Ming Tian, Changfeng Wang, Xiaoming Hu, Ran Cheng and Yi Zhao (<i>College of Information Science & Electronic Engineering, Zhejiang University; Shanghai Huali Microelectronics Corporation</i>)
D2-5	0461: Design and Analysis of high robustness dual- direction SCR with heavily doping in NW
17: 15	Zijie Zhou, Xiangliang Jin, Yang Wang (<i>School of Physics and Optoelectronics, Xiangtan University; School of Physics and Electronics, Hunan Normal University</i>)
D2-6	0492: Dual-Threshold Independent-Gate TFET with Tri-side Tunneling
17: 30	Pengfeng Zhang, Jianping Hu (<i>Faculty of Information Science and Technology, Ningbo University</i>)

Wednesday, October 30, 17: 45 – 18: 45

Wednesday, October 30, 17: 45 – 18: 45

Poster Session I

Hotel Hilton 3rd Floor

Session Chair : Min Liu

	Title
P1-1	0302: Design of High Dynamic Range and Digitalized Readout Integrated Circuit

	for LWIR FPAs
	JunQiao, Xiao Wang, Yaohong Zhao (<i>Shenyang Institute of Automation, Chinese Academy of Sciences; Key Laboratory of Opto-Electronic Information Processing, Chinese Academy of Sciences</i>)
P1-2	0304: Near-Threshold and Fast-Locking All-Digital Environmental Variation-Aware SARDLL
	Tailong Xu, Chao Xu, Xueyou Hu (<i>Key Laboratory of Intelligent Computing & Signal Processing, Ministry of Education, Anhui University; Department of Electronic Information and Electrical Engineering, Hefei University</i>)
P1-3	0306: A 5-bit, 87-fs Step, Constant-Slope, Charge-Sharing-Based Encoding Digital-to-Time Converter in 130nm CMOS
	Junyao Wang, Hairui Wang and Bo Wang (<i>The Key lab of IMS, School of ECE, Peking University Shenzhen Graduate School</i>)
P1-4	0314: A 96kb, 0.36V, Energy-Efficient 8T-SRAM with Column-Selection and Shared Buffer-Foot Techniques for EEG Processor
	Liang Wen, Yu Liu, Wei Mo, Jing Zhang, Shiqian Qi, Jianping Lv, Yuejun Zhang (<i>Department of Electronic Technology, China Coast Guard Academy; Department of Warship Command, China Coast Guard Academy</i>)
P1-5	0325: A radiation resistant library based on DICE and fault-tolerant delay filtering techniques in CMOS 0.18μm technology
	Yongsheng Wang, Yanyan Gao, Feng Chong, Nan Zhang (<i>Department of Microelectronics, Harbin Institute of Technology</i>)
P1-6	0326: A Micro Power High Precision Sigma-Delta ADC with Adjustable Decimation Ratio
	Yongsheng Wang, Anyi Wang, Lei Li, Chengxin Zhao (<i>Department of Microelectronics, Harbin Institute of Technology</i>)
P1-7	0346: A design of a wideband balanced limited low noise amplifier
	Li Ming, ZengZhi, Wei Hongtao (<i>The 13th Research Institute of CHINA Electronics Technology Group Corporation</i>)
P1-8	0367: A 20GS/s Track-and-Hold Amplifier based on InP DHBT Process
	Jian Gong, ZiRun Zhao, ZiQing Wang, YongHui Wu, Yong Cui (<i>The 13th Research Institute of China Electronics Technology Group Corporation</i>)
P1-9	0388: Ultra-Low-Power CMOS Temperature Sensor for UHF RFID Systems
	Kun Peng, Yong Xu, Mingqian Sun (<i>Institute of Communication Engineering, Army Engineering University of PLA</i>)

P1-10	0412: A FT Trimming Circuit Based on EPROM and Pin Multiplexing
	Yan-Ming Li, Xiao-Xiao Wang, Xiao-Li Xi, Jian Sun, Zhong-Hui Chen (<i>School of Electronic and Control Engineering, Chang ' an University</i>)
P1-11	0422: A Low-power, High-reliability STT-MRAM Write Scheme with Real-time Voltage Sensing Module
	Hao Li, Hongmei Yu, Dongsheng Liu, Peng Liu, Bo Liu (<i>School of Optical and Electronic Information, Huazhong University of Science and Technology; Zhejiang Hikstor Technology Co., Ltd., Hangzhou</i>)
P1-12	0455: A Low- Power Single-Slope based 14-bit Column-Level ADC for 384×288 Uncooled Infrared Imager
	Xueyou Shi, Dahe Liu, Zhongjian Chen, Guangyi Chen, Shoudong Huang and Wengao Lu, Yacong Zhang (<i>Peking University Shenzhen Graduate School; National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Peking University</i>)
P1-13	0476: A 35μW Receiver Front-End with 35% wireless energy harvesting efficiency for Wearable Medical Applications
	Zirui Jin, Ang Hu, Zilong Liu, Dongsheng Liu (<i>School of Optical and Electronic information, Huazhong University of Science and Technology</i>)
P1-14	0484: An On-Time Generator with Zero Quiescent Power Consumption Suitable for AOT Buck Converters
	Zekun Zhou, Zhengyang Jin, Jianwen Cao, Yue Shi, Bo Zhang (<i>State key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China; College of Communication Engineering, Chengdu University of Information Technology</i>)
P1-15	0500: A Readout Circuit of Microchannel Plate Light Detector in 0.13μm CMOS Technology
	Haoran Gong, Yunhao Fu, Ning Ding, Jiaqi Jiang, Yuchun Chang (<i>College of Electronic Science and Engineering, Jilin University</i>)
P1-16	0533: Influences of the Source and Drain Resistance of the MOSFETs on the Single Event Upset Hardness of SRAM cells
	Zhongshan Zheng, Zhentao Li, Bo Li, Jiajun Luo, Zhengsheng Han (<i>Institute of Microelectronics, Chinese Academy of Sciences; Key Laboratory of Silicon Device Technology, Chinese Academy of Sciences</i>)
P1-17	0546: A 16/32Gb/s NRZ/PAM4 Receiver with Dual-Loop CDR and Threshold Voltage Calibration
	Songhao Guo, Li Ding and Jing Jin (<i>Center for Analog/RF Integrated Circuits (CARFIC), School of Microelectronics, Shanghai Jiaotong University</i>)

P1-18	0550: A 60GHz Digitally-Controlled Differential Reflection-type Phase Shifter in 65-nm CMOS with Low Phase Error
	Wentao Lv, Xiaokang Niu, Lianming Li (<i>National Mobile Communication Research Lab, Southeast University; Purple Mountain Laboratories, Nanjing</i>)
P1-19	0631: A 60 GHz single-to-differential LNA using slow-wave CPW and transformer coupling in 28 nm CMOS
	Benqing Guo, Haifeng Liu, Yao Wang, and Jun Chen (<i>University Electronic Science and Technique of China; Chengdu University</i>)
P1-20	0633: A 0.0558-mm² 0.05-0.9GHz Low-Power Multi-phase Non-overlap Clock Generator in 40 nm CMOS
	Zhigang Li, Xiaofei Wang, and Jing Jin (<i>Center for Analog/RF Integrated Circuits (CARFIC), School of Microelectronics, Shanghai Jiaotong University</i>)
P1-21	0648: An 8-12GHz Class-F3 VCO with Multi-LC Tank in 28nm CMOS
	Tao Wang, Wei Li, Haoyang Zhou, Jiao Ye, Yuanyuan Xu (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
P1-22	0651: An Optimized Modeling Method for Transformer Design
	Yingying Liang, Xiaoming Liu, and Jing Jin (<i>Center for Analog/RF Integrated Circuits (CARFIC), School of Microelectronics, Shanghai Jiaotong University</i>)
P1-23	0659: Low-Dropout Regulator design with a simple structure for good high frequency PSRR performance based on Bandgap Circuit
	Xiaozhi Kang, Xiaoxu Kang, Zijian Zhao, Jingxiu Ding, Yi Hu, Dapeng Xu, Qingqing Sun, David Wei Zhang (<i>State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University; Process Technology Department, Shanghai IC R&D Center</i>)
P1-24	0663: Design of an Adaptive Loop Gain Controller Based on Auto-correlation Detection Scheme in All-Digital Phase-Locked Loop
	Sheng Zhang, Song Jia, Hanzun Zhang, Rongshan Wei, Weixin Gai (<i>College of Physics and Information Engineering, Fuzhou University; Key Laboratory of Microelectronics Devices and Circuits (MOE), Institute of Microelectronics, Peking University</i>)
P1-25	0666: A High-Linear Digital-to-Phase Converter in 40nm CMOS
	Yu Ji, Li Ding, and Jing Jin (<i>School of Microelectronics, Shanghai Jiao Tong University</i>)
P1-26	0676: Architecture considerations of LTE/WCDMA wideband power amplifier for efficiency improvement
	Abdulraqeb Abdullah Saeed Abdo, Jie Ling, Pinghua Chen (<i>Faculty of Computer,</i>

	<i>Guangdong University of Technology)</i>
P1-27	0680: An FPGA based verification platform for pipeline ADC digital calibration technology
	Yuehong Gong, Min Luo, MingyuWang (<i>Naval Architecture & Marine Engineering College, Shandong Jiaotong University; Microelectronic R&D Center, Harbin Institute of Technology in Weihai</i>)
P1-28	0691: An Automatic Slope-Calibrated Ramp Generator for Single-Slope ADCs
	Shoudong Huang, Wengao Lu, Ye Zhou, Shanzhe Yu, Yacong Zhang, Xueyou Shi, Zhongjian Chen (<i>Key Laboratory of Microelectronic Devices and Circuits, Institute of Microelectronics, Peking University</i>)
P1-29	0692: A Sub-1dB NF Receiver for 1.5T Magnetic Resonance Imaging
	Chang Yu, Xiaojing Lv, Yanhui Li, and Tingting Mo (<i>School of Electronic Information and Electrical Engineering Shanghai Jiao Tong University</i>)
P1-30	0713: A 1.26-ps-FoM Output-Capacitorless LDO with Dual-Path Active-Feedback Frequency Compensation and Current-Reused Dynamic Biasing in 65-nm CMOS Technology
	Huimin Qian and Jianping Guo (<i>School of Electronics and Information Technology, Sun Yat-Sen University</i>)
P1-31	0795: A Double-Latch Comparator for Multi-GS/s SAR ADCs in 28nm CMOS
	Pingshun Ma, Yongzhen Chen, and Jiangfeng Wu (<i>Tongji University</i>)
P1-32	0718: A Calibration Technique for Two-Step Single-Slope Analog-to-Digital Converter
	Wenjie Huang, Qihui Zhang, Jing Li, Zhong Zhang, Heng Deng, Ning Ning, Qi Yu (<i>School of Electronic Science and Engineering, University of Electronic Science and Technology of China</i>)
P1-33	0720: A Comparator-Reused Dynamic-Amplifier for Noise-Shaping SAR ADC
	Longheng Luo, Xingchen Shen, Jianguo Diao, Fan Ye, Junyan Ren (<i>State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University</i>)
P1-34	0728: A CMOS Half-Bridge GaN Driver with 6-30V Input Voltage Range and 5.4ns Propagation Delay
	Haosheng Zeng, Hong Zhang, and Jianping Guo (<i>School of Electronics and Information Technology, Sun Yat-sen University</i>)
P1-35	0734: 12.5GHz clock generator for 4x100Gbps high speed serial interface
	Kewei Xin, Fangxu Lv, Jianye Wan, Heming Wang, Kaile Guo, Yuxuan Wu (<i>Air and Missile Defense College, Air Force Engineering University</i>)

P1-36	0738: A 22-40.5 GHz UWB LNA Design in 0.15um GaAs
	Dong Wei, Jincheng Zhang, Tianxiang Wu, Shunli Ma, Junyan Ren (<i>School of Microelectronics, Fudan University</i>)
P1-37	0742: A 256MHz Analog Baseband Chain with tunable Bandwidth and Gain for UWB Receivers
	Yuting Yao, Jipeng Wei, Manxin Li, Shunli Ma, Fan Ye, Junyan Ren (<i>State-key Laboratory of ASIC and System, Fudan University</i>)
P1-38	0749: A 130-150 GHz Power Amplifier for Millimeter Wave Imaging in 65-nm CMOS
	Jincheng Zhang, Lihe Nie, Dong Wei, Tianxiang Wu, Shunli Ma, Junyan Ren (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
P1-39	0754: A 36-40 GHz VCO with bonding inductors for millimeter wave 5G Communication
	Tianxiang Wu, Jincheng Zhang, Dong Wei, Lihe Nie, Yuting Yao, Shunli Ma, Junyan Ren (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
P1-40	0758: A 63.3ps TDC Measurement System Based on FPGA for Pulsed Laser Ranging
	Zhiyong Chen, Weiwei Shi, Guoqiang Xiong, Junwei Yang, Yuan Xu (<i>School of Information and Electronics Engineering, Shenzhen University</i>)
P1-41	0764: A Power-Area-Efficient Low-Dropout Regulator With Enhanced Buffer Impedance Attenuation
	Ziyun He, Shaoquan Liao, Zixin Wang, Jianping Guo (<i>School of Microelectronics and Information Technology, Sun Yat-sen University</i>)

Thursday

Thursday, October 31, 8: 30 – 10: 00

Thursday, October 31, 8: 30 – 10: 00

Grand Ball Room

Keynote Session K3

Hotel Hilton 3rd Floor

Session Chair : Hidetoshi Onodera

K3-1 The Cognitive Edge (8: 30-9: 15)

Prof. Jan M. Rabaey, UC Berkeley, USA; CTO & STCO, IMEC, Belgium

K3-2 ESD protection circuits for CMOS technology (9: 15-10: 00)

Dr. Teruo Suzuki, Socionext Inc., Japan

Thursday, October 31, 10: 15 – 12: 15

Thursday, October 31, 10: 15 – 12: 15	Xi'An+Dalian Room
Special Session A3 : Efficient Digital Designs & Applications	
	Hotel Hilton 4 th Floor
Session Chair : Chuan Zhang	

	Title
A3-1	0805: Training Adaptive Hardware for Reconfigurability: A Simplified Case Study (Invited Paper)
10: 15	Chongzhou Fang, Zaichen Zhang, Xiaohu You and Chuan Zhang (<i>Lab of Efficient Architectures for Digital-communication and Signal-processing (LEADS); National Mobile Communications Research Laboratory, Southeast University</i>)
A3-2	0803: A Fast Signal Integrity Design Model of Printed Circuit Board based on Monte-Carlo Tree (Invited Paper)
10: 39	Tingrui Zhang, Siyu Chen, Shuwu Wei, and Jienan Chen (<i>University of Electronic Science and Technology of China</i>)
A3-3	0804: ANN Based Adaptive Successive Cancellation List Decoder for Polar Codes (Invited Paper)
11:03	Wenqing Song, Yuxiang Fu, Qinyu Chen, Li Li, Chuan Zhang (<i>School of Electronic Science and Engineering, Nanjing University; Lab of Efficient Architectures for Digital-communication and Signal-processing (LEADS)</i>)
A3-4	0801: A Novel Signed Bit-serial Fixed-point Accumulator with Configurable Overflow-Protection Precision (Invited Paper)
11: 27	Lin Li, Qiu Huang, Jienan Chen, Jianhao Hu (<i>National Key Laboratory of Science and Technology on Communications, University of Electronic Science and Technology of China</i>)
A3-5	0809: Redundancy-Aided Iterative Reliability-Based Majority-Logic Decoding for NB-LDPC Codes (Invited Paper)
11: 51	Suwen Song, Jing Tian, Jun Lin, Zhongfeng Wang (<i>School of Electronic Science and Engineering, Nanjing University</i>)

Thursday, October 31, 10: 15 – 12: 15	Wuhan+Nanjing Room
Session B3 : Computing-in/near-Memory II	
Session Chair : Tzu-Hsien Sang	

	Title
B3-1	0807: Area-Efficient Distributed Arithmetic Optimization via Heuristic Decomposition and In-Memory Computing (Invited Paper)
10: 15	Jian Chen, Wenfeng Zhao, Yajun Ha (<i>School of Information and Science Technology,</i>

	<i>Shanghaitech University, Shanghai, China; Department of Biomedical Engineering, University of Minnesota, Minneapolis, MN, USA)</i>
B3-2	0789: Flash-based Computing in-Memory Scheme for IOT (Invited Paper)
10: 45	J.F. Kang, P. Huang, R.Z. Han, Y.C. Xiang, X.L. Cui, X.Y. Liu (<i>Department of Microelectronics, Peking University; Key Laboratory of Integrated Microsystems, Peking University Shenzhen Graduate School</i>)
B3-3	0566: A Low-Power High-Throughput In-Memory CMOS-ReRAM Accelerator for Large-Scale Deep Residual Neural Networks (Invited Paper)
11: 15	Yuan Cheng, Ngai Wong, Xiong Liu, Leibin Ni, Hai-Bao Chen, Hao Yu (<i>Department of Micro/Nano Electronics, Shanghai Jiao Tong University; Department of Electrical and Electronic Engineering, The University of Hong Kong</i>)

Thursday, October 31, 10: 15 – 12: 15	Happiness Room
Session C3 : DAC & other Data Converter Module	Hotel Hilton 3 rd Floor
Session Chair : Tai-Cheng Lee	

	Title
C3-1	0693: Fine Time Resolution TDC Architectures -Integral and Delta-Sigma Types (Invited Paper)
10: 15	Haruo Kobayashi, Kosuke Machida, Yuto Sasaki, Yusuke Osawa Pengfei Zhang, Lei Sha, Yuki Ozawa, Anna Kuwana (<i>Division of Electronics and Informatics, Graduate School of Science and Technology, Gunma University</i>)
C3-2	0808: High Linear Ring Amplifier Design with Analysis on Settling Procedures (Invited Paper)
10: 45	Yongzheng Chen (<i>Electronic and information engineering college, Tongji University, Shanghai</i>)
C3-3	0448: A Low-Temperature-Coefficient and High-PSRR Bandgap Reference for Readout Circuit of SPAD
11: 15	Xuefeng Ye, Duoduo Zeng, Xiangliang Jin, Yang Wang (<i>School of Physics and Optoelectronics, Xiangtan University; Hunan Engineering Laboratory for Microelectronics, Optoelectronics and System on a Chip</i>)
C3-4	0650: Systematic Construction of Resistor Ladder Network for N-ary DACs
11: 27	Manato Hirai, Shuhei Yamamoto, Hirotaka Arai, Anna Kuwana1, Hiroshi Tanimoto, Yuji Gendai, Haruo Kobayashi (<i>Division of Electronics and Informatics, Faculty of Science and Technology, Gunma University; Kitami Institute of Technology</i>)
C3-5	0681: A High Reliability 500 μW Resistance-to-Digital Interface Circuit for SnO₂ Gas Sensor IoT Applications
11: 39	Jianguo Yang, Xiaoyong Xue, Xiaoxin Xu, Hangbing Lv, Ming Liu (<i>Key Laboratory</i>

	<i>of Microelectronics Devices and Integrated Technology, Institute of Microelectronics of the Chinese Academy of Sciences; ASIC and System State Key Laboratory, School of Microelectronics, Fudan University)</i>
C3-6	0399: A curvature corrected bandgap reference with mismatch cancelling and noise reduction
11: 51	Dehong Lv, Heng Ma, Fuqiang Liu, Zhiliang Hong (<i>School of Microelectronics, Fudan University, Shanghai</i>)
C3-7	0642: A Low-Power 10-bit 160-MSample/s DAC in 40-nm CMOS for Baseband Wireless Transmitter
12: 03	Yifei Wang, Xiaofei Wang, Yuekang Guo and Jing Jin (<i>Center for Analog/RF Integrated Circuits (CARFIC), School of Microelectronics Shanghai Jiaotong University</i>)

Thursday, October 31, 10: 15 – 12: 15	Fortune Room
Session D3 : Device Simulation & Integration II	Hotel Hilton 3 rd Floor
Session Chair : Pei-Wen Li	

	Title
D3-1	0333: Monolithically Integrated Inverter using AlGaIn/GaN-based Depletion-Mode and Enhancement-Mode Metal-Oxide-Semiconductor High Electron Mobility Transistors (Invited Paper)
10: 15	Ching-Ting Lee and Hsin-Ying Lee (<i>Department of Electrical Engineering, Yuan Ze University; Department of Photonics, National Cheng Kung University</i>)
D3-2	0374: A Platform with Exquisite Film Profile Engineering in Oxide-Based Thin-Film Transistors for More-than-Moore Applications (Invited Paper)
10: 42	Horng-Chih Lin and Yu-An Huang (<i>Institute of Electronics, National Chiao Tung University</i>)
D3-3	0646: Addressing Aging Issues in Heterogeneous Three-Dimensional Integrated Circuits (Invited Paper)
11: 09	Yu Ma, Dingcheng Jia, Wei Gao and Pingqiang Zhou (<i>School of Information Science and Technology, ShanghaiTech University</i>)
D3-4	0767: Applications and Schemes based on 3D Heterogeneous Integration (Invited Paper, abstract only)
11: 36	Kuan-Neng Chen (<i>National Chiao Tung University</i>)
D3-5	0467: MoS2 transistor gated by PMMA-based electrolyte for Sub-1V Operation
12: 03	Hongwei Tang, Fuyou Liao, Xinzhi Zhang, Jianan Deng, Jing Wan, Wenzhong Bao (<i>State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University; State Key Laboratory of ASIC and System, School of Information Science and Engineering, Fudan University</i>)

Thursday, October 31, 13: 30 – 15: 30

Thursday, October 31, 13: 30 – 15: 30	Xi'An+Dalian Room
Special Session A4: Smart Circuit and System I	Hotel Hilton 4 th Floor
Session Chair : Sujuan Liu	

	Title
A4-1	0752: Efficient Photometric Alignment for Around View Monitor System (Invited Paper)
13: 30	Cong Lai, Guangyu Wang, Qingyu Yang, Hongbin Sun (<i>Xi'an Jiaotong University</i>)
A4-2	0408: A Variation Aware Register Clustering Methodology in Near-Threshold Region (Invited Paper)
13:45	Xiangnan Song, Shiyang Zhang, Ju Zhou, Xuexiang Wang (<i>National ASIC System Engineering Research Center, Southeast University; College of Software Engineering (Suzhou), Southeast University</i>)
A4-3	0511: An Ultra-Low Power Cycle-by-Cycle Current Limiter Suitable for Switching-Mode Power Supply with 2.2 MHz Frequency (Invited Paper)
14: 15	Yue Shi, Jiawen Wang, Jianwen Cao, Zekun Zhou (<i>College of Communication Engineering, Chengdu University of Information Technology; State key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China</i>)
A4-4	0405: Buffer Sizing for Near-Threshold Clock Tree using Improved Genetic Algorithm (Invited Paper)
14:30	Yiran Sun, Ju Zhou, Shiyang Zhang, Xuexiang Wang (<i>National ASIC System Engineering Research Center, Southeast University; College of Software Engineering (Suzhou), Southeast University</i>)

Thursday, October 31, 13: 30 – 15: 30	Wuhan+Nanjing Room
Session B4 : Memory & MEMS I	Hotel Hilton 4 th Floor
Session Chair : Alan Seabaugh	

	Title
B4-1	0791: On the possibility of incorporating Si MOSFETs with surface plasmon for integrated biosensing applications (Invited Paper, abstract only)
13: 30	Jun Liu and Ya-Hong Xie (<i>Department of Materials Sciences & Engineering, University of California, Los Angeles</i>)
B4-2	0787: The Advances of OTP Memory for Embedded Applications in HKMG CMOS Generation and Beyond (Invited Paper)

14: 00	Steve S. Chung (<i>Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University</i>)
B4-3	0356: Graphene Biosensor for Saliva Protein Adsorption
14:30	Shiyu Wang, Md. Zakir Hossain, Takaaki Suzuki, Kazuo Shinozuka, Natsuhiko Shimizu, Shunya Kitada, Ryo Ichige, Anna Kuwana, Haruo Kobayashi (<i>Faculty of Science and Technology, Gunma University</i>)
B4-4	0544: Development and Optimization of Contact Module Process for Micro-Bridge Structure based MEMS/Sensor Application
14:45	Xiaoxu Kang, Xiaolan Zhong, Ming Li (<i>Process Technology Department, Shanghai IC R&D Center</i>)

Thursday, October 31, 13: 30 – 15: 30	Happiness Room Hotel Hilton 3 rd Floor
Session C4 : RF Circuit	
Session Chair : Kiat Seng Yeo	

	Title
C4-1	0510: Ultrahigh-Speed One-Chip CMOS Transceiver with 300-GHz Band (Invited Paper)
13: 30	Minoru Fujishima (<i>Graduate School of Frontier Sciences of Matter, Hiroshima University</i>)
C4-2	0798: Reconfigurable RF Power Amplifier in 5G/4G with RF-SOI CMOS (Invited Paper)
13: 55	Yang Yang Peng, Ping Li , Yang Li (<i>SmarterMicro</i>)
C4-3	0522: A 0.9/1.8/2.4GHz-reconfigurable LNA with Inductor and Capacitor Tuning for IoT Application in 65nm CMOS
14: 20	Xinpeng Xing, Pengyi Cao, Haigang Feng and Zhihua Wang (<i>Graduate School at Shenzhen, Tsinghua University, Shenzhen; Institute of Microelectronics, Tsinghua University</i>)
C4-4	0426: One-channel Zero-IF Multi-mode GNSS Receiver with Self-adaptive Digitally-assisted Calibration
14: 34	Li Songting, Lihu Chen, Yong Zhao (<i>College of Aerospace Science and Engineering, National University of Defense Technology</i>)
C4-5	0516: The Design and Performance Comparison of Wide Bandwidth LNA with Three Different Kinds of Technologies
14: 48	Huashu Wang, Wei Ma, Zhiming Xiao, Wei-Chih Cheng, Liang Wang, Fanming Zeng, Hongyu Yu and Weibo Hu (<i>College of Electronic Information and Optical Engineering, NanKai University; Nankai University Shenzhen Graduate School, Nankai University</i>)

C4-6	0366: A 35.2 dBm CMOS RF Power Amplifier Using an 8-Way Current-Voltage Combining Transformer with Harmonic Control
15: 02	HejiaCai, Yan Hu, Zhiliang Hong (<i>State Key Laboratory of ASIC & System, Fudan University</i>)
C4-7	0371: A Compact Quadrature Doherty Digital Power Amplifier with Backoff Efficiency Enhancement
15: 16	Tao Wang, Hejia Cai, Yan Hu, Pan Xue, Zhiliang Hong (<i>State Key Laboratory of ASIC and System, Fudan University</i>)

Thursday, October 31, 13: 30 – 15: 30	Happiness Room
Session D4 : Device Simulation & Integration III	Hotel Hilton 3 rd Floor
Session Chair : Kazuhiko Endo	

	Title
D4-1	0765: OMI/TMI-based Modeling and Fast Simulation of Random Telegraph Noise (RTN) in Advanced Logic Devices and Circuits (Invited Paper)
13: 30	Runsheng Wang, Zhe Zhang, Shaofeng Guo, Qingxue Wang, Dehuang Wu, Joddy Wang, Ru Huang (<i>Institute of Microelectronics, PekingUniversity; Synopsys, Inc.</i>)
D4-2	0319: An Improved InP HEMT Small Signal Model with RC Network (Invited Paper)
14: 00	Shixing Qiao, Hongliang Lv, Yuming Zhang, Yimen Zhang, Peng Ding (<i>School of Microelectronics, Xidian University, Key Laboratory of Wide Band-Gap Semiconductor Technology; Institute of Microelectronics of Chinese Academy of Sciences</i>)
D4-3	0548: Simulation Study of Trench IGBT with Diode-Clamped P-Well for High dI/dt and dV/dt Controllability
14: 30	Rongxin Chen, Bo Yi, Moufu Kong, Xingbi Chen (<i>School of Electronic Science and Engineering, University of Electronic Science and Technology of China</i>)
D4-4	0731: A Optimized PPD CMOS Pixel with 26.09% Transfer Efficiency Improvement and 43.34% Crosstalk Suppression for I-ToF Application
14: 45	Junwei Yang, Weiwei Shi, Zhiyu Huang, Yuan Xuy, Yanghao Zheng, Xuanbin Fang (<i>School of Information and Electronics Engineering, Shenzhen University; College of Big Data and Internet, Shenzhen Technology University</i>)
D4-5	0409: Scalable Modeling for the CPW Gap Discontinuity at Frequency up to 150 GHz
15:00	Hao Sun, Jun Fu, Wenpu Cui, Tianling Ren, LinLin Liu, Wei Zhou, Quan Wang, Ao Guo (<i>Tsinghua National Laboratory for Information Science and Technology; Institute of Microelectronics, Tsinghua University</i>)

D4-6	0469: Simulation Study on Novel High Voltage Transient Voltage Suppression Diodes
15:15	Cong Liu, Moufu Kong, Hanzhi Chen, Bo Yi, Bingke Zhang (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China</i>)

Thursday, October 31, 15: 45 – 17: 45	
Thursday, October 31, 15: 45 – 17: 45	Xi'An+Dalian Room
Special Session A5: Smart Circuit and System II	Hotel Hilton 4 th Floor
Session Chair : Xuexiang Wang	

	Title
A5-1	0576: RF Transceiver System Design: From Protocols to Specifications (Invited Paper)
15: 45	Ang Hu, Dongsheng Liu, Zirui Jin, Cong Zhang, Kefeng Zhang, Lanqi Liu (<i>School of Optical and Electronic Information, Huazhong University of Science and Technology</i>)
A5-2	0574: A Hardware-efficient Accelerator for Encoding Stage of Text-to-speech Synthesis (Invited Paper)
16: 09	Riyong Zheng, Chenghao Wang, Jun Han, Xiaoyang Zeng (<i>School of Microelectronics, Fudan University; State Key Laboratory of ASIC and System, Fudan University</i>)
A5-3	0744: High throughput multi-code LDPC encoder for CCSDS standard (Invited Paper)
16: 33	Jinfou Xie, Shixian Li, Yun Chen, Qichen Zhang, Xiaoyang Zeng (<i>State Key Lab of ASIC & System, Fudan University</i>)
A5-4	0753: MMV Subspace Pursuit (M-SP) Algorithm for Joint Sparse Multiple Measurement Vectors Recovery (Invited Paper)
16: 57	Sujuan Liu, Lili Zheng, Lei Liu, Qianjin Lin (<i>School of Microelectronics, Beijing University of Technology</i>)
A5-5	0398: Deep Spiking Convolutional Neural Networks for Programmable Neuro-synaptic System (Invited Paper)
17: 21	Chenglong Zou, Xinan Wang, Boxing Xu, Yisong Kuang, Xiaoxin Cui (<i>Key Laboratory of Integrated Microsystem, School of ECE, Peking University Shenzhen Graduate School; Key Laboratory of Microelectronics Devices and Circuits, Institute of Microelectronics, Peking University</i>)

Thursday, October 31, 15: 45 – 17: 45

Session B5 : Memory & MEMS II

Session Chair : Jianguo Yang

Wuhan+Nanjing Room

Hotel Hilton 4th Floor

	Title
B5-1	0790: Dynamics of Ferroelectric and Ionic Memories: Physics and Applications (Invited Paper)
15: 45	Alan Seabaugh, Paolo Paletti, Anwesha Palit, Karla González – Serrano, and Pratyush Pandey (<i>Department of Electrical Engineering, University of Notre Dame</i>)
B5-2	0573: Advanced Simulation of RRAM Memory Cells (Invited Paper)
16: 10	Toufik Sadi, Oves Badami, Vihar Georgiev, Jie Ding and Asen Asenov (<i>Engineered Nanosystems Group, School of Science, Aalto University; School of Engineering, Electronic and Nanoscale Engineering, University of Glasgow</i>)
B5-3	0571: Evaluating the Energy Efficiency of STT-MRAMs Based on Perpendicular MTJs with Double Reference Layers (Invited Paper)
16: 35	Marco Lanuzza, Raffaele De Rose, Esteban Garzón, Felice Crupi (<i>DIMES, University of Calabria</i>)
B5-4	0641: 3D Vertical RRAM Array and Device Co-design with Physics-based Spice Model
17: 00	Weijie Xu, Yudi Zhao, Peng Huang, Xiaoyan Liu, Jinfeng Kang (<i>School of ECE, Peking University Shenzhen Graduate School; Institute of Microelectronics, Peking University</i>)
B5-5	0485: Carbon-Based Three-Dimensional SRAM Cell with Minimum Inter-Layer Area Skew Considering Process imperfections
17: 15	Jiachen Jiang, Yanan Sun, Weifeng He, Zhigang Mao, and Volkan Kursun (<i>Department of Micro-Nano Electronics, Shanghai Jiao Tong University; Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology</i>)
B5-6	0645: A Compact Memory Structure based on 2T1R Against Single-Event Upset in RRAM Arrays
17: 30	Yu Ma, Dingcheng Jia, Huifan Zhang, Ruoyu Wang and Pingqiang Zhou (<i>School of Information Science and Technology, Shanghaitech University</i>)

Thursday, October 31, 15: 45 – 17: 45

Session C5 : Wireless & Energy Harvesting Circuit

Session Chair : Minoru Fujishima

Happiness Room

Hotel Hilton 3rd Floor

	Title
C5-1	0569: Design Considerations on Integrated Rectifiers with High Efficiency and

	Wide Input Power Range for RF Energy Harvesting (Invited Paper)
15: 45	Mo Huang, Tingxu Hu, Xiuyin Zhang, Yan Lu (<i>The School of Electronic and Information Engineering, South China University of Technology, Guangzhou; Institute of Microelectronics / State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau</i>)
C5-2	0369: An Inductorless 5-GHz Differential Dual Regulated Cross-Cascode Transimpedance Amplifier using 40 nm CMOS (Invited Paper)
16: 15	Samuel Bai Song Lee, Hang Liu, Xiaopeng Yu, Jer-Ming Chen, Kiat Seng Yeo (<i>Singapore University of Technology and Design, Singapore; Zhejiang University</i>)
C5-3	0657: A UHF Semi-Passive RFID System with Photovoltaic/Thermoelectric Energy Harvesting for Wireless Sensor Networks
16: 45	Peiqing Han, Niansong Mei and Zhaofeng Zhang (<i>Shanghai Advanced Research Institute, Chinese Academy of Sciences; University of Chinese Academy of Sciences</i>)
C5-4	0402: High precision low power CMOS bandgap for RFID
17: 00	Xian Zhang, Yong Xu (<i>Institute of Communication Engineering, Army Engineering University of PLA, Nanjing, China</i>)
C5-5	0665: Dual-Loop-Controlled AC-Coupling 100MHz Bandwidth Envelope Tracking Modulator for 5G RF Power Amplifier
17: 15	Fuqiang Liu, Mingfeng Chen, Heng Ma, Zhiliang Hong (<i>School of Microelectronics, Fudan University</i>)
C5-6	0644: High-Bandwidth Wide-Output-Swing Linear Amplifier for LTE-100MHz Envelope Tracking
17: 30	Mingfeng Chen, Fuqiang Liu, Heng Ma, Zhiliang Hong (<i>School of Microelectronics, Fudan University</i>)

Thursday, October 31, 15: 45 – 17: 45

Session D5 : Novel Device

Session Chair : Eddy Simoen

Fortune Room
Hotel Hilton 3rd Floor

	Title
D5-1	0785: Monolithic Co-integration of III-V Materials into Foundry Si-CMOS in a Single Chip for Novel Integrated Circuits (Invited Paper)
15: 45	Xing Zhou, Siau Ben Chiah, Binit Syamal, and Kenneth Lee (<i>School of Electrical and Electronic Engineering, Nanyang Technological University; Low Energy Electronic Systems, SMART</i>)
D5-2	0351: Nanoscale Devices for the end of the Roadmap (Invited Paper)
16: 09	Francis Balestra (<i>Univ. Grenoble Alpes, CNRS, Grenoble INP, IMEP-LAHC</i>)

D5-3	0395: Ultra-low power consumption Spintronics Devices (Invited Paper)
16: 33	Zongxia Guo, Kaihua Cao, Kewen Shi, Weisheng Zhao (<i>Fert Beijing Institute, Beihang University; School of Microelectronics, Beihang University</i>)
D5-4	0568: Tunable diameter and interspace of Ge quantum dots for Qu bits and Readout Devices using highly controllable spacers and selective oxidation of SiGe (Invited Paper)
16: 57	Pei-Wen Li, Tsung-Lin Huang, Kang-Ping Peng, Horng-Chih Lin, and Tom George (<i>Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan</i>)
D5-5	0390: Post-Si Nano Device Technology (Invited Paper)
17: 21	Kazuhiko Endo (<i>Nanoelectronics Research Institute, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan</i>)

Thursday, October 31, 17: 45 – 18: 45

Thursday, October 31, 17: 45 – 18: 45

Poster Session II

Hotel Hilton 3rd Floor

Session Chair : Yi Zhao

	Title
P2-1	0315: A Low On-state Voltage and Large Current Capability Thin SOI-LIGBT with Trench NMOS
	Jun Huang, Moufu Kong, Xing Bi Chen (<i>State Key Laboratory of Electronic Thin Films and Integrated Devices, University of Electronic Science and Technology of China</i>)
P2-2	0316: Analysis and Optimal Design of a New Single-Photon Memristor
	PENG Bo, JIN Xiang-Liang (<i>School of Physics and Optoelectronics, Xiangtan University; School of Physics and Electronics, Hunan Normal University</i>)
P2-3	0800: Inverse RIE micro-loading in deep etching of silicon via array
	Xubo Wang, Qing Wang, Jia Zhou (<i>School of Microelectronics, Fudan University</i>)
P2-4	0330: Improved Model for ESD Failure Caused by Stressing No Connect Pin
	Jingrui Ma, Qi-an Xu, Blacksmith Wu, Kanyu Cao (<i>Product Research and Development, ChangXin Memory Technologies, Inc.</i>)
P2-5	0375: A Method to Design 5-Bit Burst Error Correction Code against the Multiple Bit Upset (MBU) in Memories
	Jia-Qiang Li, Li-Yi Xiao, Liu He, Hao-Tian Wu (<i>Microelectronics Center, Harbin Institute of Technology</i>)

P2-6	0397: An Obfuscated Challenge Design for APUF to Resist Machine Learning Attacks
	Bo Chen, Pengjun Wang, Gang Li (<i>College of Electrical and Electronic Engineering, Wenzhou University; Faculty of Electrical Engineering and Computer Science, Ningbo University</i>)
P2-7	0406: Circuit-Level Soft Error Rate Evaluation Approach Considering Single-Event Multiple Transient
	Xiaoyu Zhang, Bin Liang, Ruiqiang Song (<i>College of Computer, National University of Defense Technology</i>)
P2-8	0418: UVM-based Functional Coverage Driven AXI4-stream Verification
	Chunlin Xu, Wei Ni, Yukun Song (<i>Institute of VLSI Design, Hefei University of Technology</i>)
P2-9	0419: A GaSb/In_{0.4}Ga_{0.6}As Heterojunction Z-Shaped Tunnel Field-Effect Transistor with High Performance
	Jiarui Bao, Shuyan Hu, Guangxi Hu, Laigui Hu, Ran Liu, and Lirong Zheng (<i>State Key Laboratory of ASIC & System, School of Information Science and Technology, Fudan University</i>)
P2-10	0421: A Configurable Architecture of ANN in Hardware with Resource-Efficient Reusable Neuron
	Jiahao Lu, Xianghua Luo, Dongsheng Liu, Peng Liu, Bo Liu (<i>School of Optical and Electronic Information, Huazhong University of Science and Technology; Zhejiang Hikstor Technology Co., Ltd.</i>)
P2-11	0425: Designing a 3D graphics processor for mobile applications
	Lingjuan Wu, Wenqian Zhao, Dunshan Yu (<i>College of Informatics, Huazhong Agricultural University; Institute of Microelectronics, Peking University</i>)
P2-12	0437: Learning Sparse Patterns in Deep Neural Networks
	Weijing Wen, Fan Yang, Yangfeng Su, Dian Zhou, Xuan Zeng (<i>State Key laboratory of ASIC and system, Fudan University</i>)
P2-13	0439: Scheduling Algorithm Based on System of Difference Constraints Using Network Flow
	Hao Jiang, Yang Fan and Xuan Zeng (<i>State Key laboratory of ASIC and system, Fudan University</i>)
P2-14	0442: Graphene Top-gated MoS₂ Phototransistors
	Yaochen Sheng, Xinyu Chen, Fuyou Liao, Jianan Deng, Jing Wan, Wenzhong Bao (<i>State Key Laboratory of ASIC and System, School of Microelectronics; School of</i>

	<i>Information Science and Engineering, Fudan University)</i>
P2-15	0457: Adsorbates on Multilayer Graphene Surface: Morphology, Distribution and Electrical Properties
	Muchan Li, Pei Peng, Zhongzheng Tian, Liming Ren, and Yunyi Fu (<i>Institute of Micro-/Nanoelectronics, Peking University</i>)
P2-16	0478: Collaborative Implementation of Hardware-Oriented GBDT Compress Algorithm Based on DSP+FPGA
	Yafei Li, Kuizhi Mei, Xiao Wang, Zeng Zhang, Hejie Yu (<i>School of Microelectronics, Xi'an Jiaotong University</i>)
P2-17	0482: High-speed Classification of AER Data Based on a Low-cost Hardware System
	Jinguo Huang, Yingcheng Lin, Wei He, Xichuan Zhou, Cong Shi, Nanjian Wu, Gang Luo (<i>School of Microelectronics and Communication Engineering, Chongqing University</i>)
P2-18	0504: Approximate Multiplier Using Reordered 4-2 Compressor with OR-based Error Compensation
	Yufeng Xu, Yi Guo, Shinji Kimura (<i>Graduate School of Information, Production and System, Waseda University, Japan</i>)
P2-19	0505: High-Speed ASIC Implementation of Paillier Cryptosystem with Homomorphism
	Chun Cai, Hiromitsu Awano, Makoto Ikeda (<i>EEIS, Graduate School of Engineering, The University of Tokyo; VLSI Design Education Center, The University of Tokyo</i>)
P2-20	0520: Parallel Global Placement on CPU via Parallel Reduction
	Huaidong Gao, Fan Yang, Dian Zhou and Xuan Zeng (<i>State Key Lab of ASIC & System, Fudan University</i>)
P2-21	0521: An Energy-Efficient Mixed-Signal Parallel Multiply-Accumulate (MAC) Engine Based on Stochastic Computing
	Xinyue Zhang, Jiahao Song, Yuan Wang, Yawen Zhang, Zuodong Zhang, Runsheng Wang, Ru Huang (<i>Institute of Microelectronics and Key Laboratory of Microelectronics Devices and Circuits, Peking University</i>)
P2-22	0541: Novel smart card SoC memory architecture based on embedded STT-MRAM
	Kaiwen Lu, Fengze Yan, Xingjie Liu, Dongsheng Liu, Peng Liu, Bo Liu (<i>School of Optical and Electronic Information, Huazhong University of Science and Technology; Zhejiang Hikstor Technology Co., Ltd.</i>)

P2-23	0578: Enhanced Recursive Residual Network for Single Image Super-Resolution
	Yi Zhang, Xiaoshan He, Minge Jing, Yibo Fan, Xiaoyang Zeng (<i>School of Microelectronics, Fudan University</i>)
P2-24	0582: An Efficient ASIC Implementation of Public Key Cryptography Algorithm SM2 Based on Module Arithmetic Logic Unit
	Danyang Yang, Zibin Dai, Wei Li, Tao Chen (<i>Institute of Information Science and Technology</i>)
P2-25	0668: An FPGA Implementation of GCN with Sparse Adjacency Matrix
	Luchang Ding, Zhize Huang, Gengsheng Chen (<i>School of Microelectronics, Fudan University</i>)
P2-26	0670: An FPGA-based Hardware Accelerator of RANSAC Algorithm for Matching of Images Feature Points
	Ziwei Zhao, Fei Wang, Qi Ni (<i>School of Electronics and Information Engineering, Harbin Institute of Technology</i>)
P2-27	0671: A Implementation for Built-in Self-Testing of RapidIO by JTAG
	Hu Chunmei, Zhang Zhenyang, Guo Yang, Xu Jingyanan (<i>School of Computer, National University of Defense Technology</i>)
P2-28	0682: Improve DRAM Leakage Issue During RAS Operational Phase Through TCAD Simulation
	Ning Li, Wen-Yong Jiang, Blacksmith Wu, Kanyu Cao (<i>Product Research and Development, ChangXin Memory Technologies, Inc.</i>)
P2-29	0685: 20, 000-fps Visual Motion Magnification on Pixel-parallel Vision Chip
	Junxian He, Xichuan Zhou, Yingcheng Lin, Chonglei Sun, Cong Shi, Nanjian Wu, Gang Luo (<i>School of Microelectronics and Communication Engineering, Chongqing University</i>)
P2-30	0686: A Coarse-to-fine Classification for Motion Blur Kernel Size Estimation with Cascaded Neural Networks
	Minyuan Ye, Lei He, Gengsheng Chen (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
P2-31	0689: A pn-coupled Superjunction IGBT for High Switching Speed
	Lei Liu, Yao Yao, Meng-Qi Wen, Yue Li, David Wei Zhang (<i>School of Microelectronics, Fudan University; Suzhou Oriental Semiconductor</i>)
P2-32	0694: GaN Schottky Diode Model for THz Multiplier Design with Consideration of Self-heating Effect
	Xubo Song, Yuanjie Lv, Yamin Zhang, Lisen Zhang, Shixiong Liang, Xin Tan, Shaobo

	Dun, Dabao Yang, Zhirong Zhang, Yuangang Wang, Zhihong Feng (<i>National Key Laboratory of ASIC, Hebei Semiconductor Research Institute; Laboratory of Semiconductor Device Reliability Physics, Beijing University of Technology</i>)
P2-33	0701: Nonvolatile Binary CNN Accelerator with Extremely Low Standby Power using RRAM for IoT Applications
	Yujie Cai, Keji Zhou, Xiaoyong Xue, Mingyu Wang, Xiaoyang Zeng (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
P2-34	0711: A New Approximate Multiplier Design for Digital Signal Processing
	Yue Zhao, Tong Li, Feng Dong, Qin Wang, Weifeng He, Jianfei Jiang (<i>Department of Micro/Nano Electronics, Shanghai Jiao Tong University; Beijing iQIYI Science & Technology Co., Ltd.</i>)
P2-35	0714: Study for NOR Flash cell burn out failure improvement in the advanced node below 65nm
	Peng Sun, Yum Li, Yao Yao, Peng-Fei Wang (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
P2-36	0721: Deploying and Optimizing Convolutional Neural Networks on Heterogeneous Architecture
	Junning Jiang, Liang Cai, Feng Dong, Kehua Yu, Ke Chen, Wei Qu, Jianfei Jiang (<i>School of Microelectronics, Shanghai Jiao Tong University; Beijing iQIYI Science & Technology Co., Ltd.</i>)
P2-37	0725: A digitalized RRAM-based Spiking Neuron Network system with 3-bit weight and unsupervised online learning scheme
	Danqing Wu, Shilin Yan, Haodi Tang, Yu Wang, Jiayun Feng, Xianwu Hu, Jiaxin Cao, Yufeng Xie (<i>State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University</i>)
P2-38	0732: Hardware Implementation of Convolutional Neural Network for Face Feature Extraction
	Ru Ding, Xuemei Tian, Guoqiang Bai, Guangda Su, Xingjun Wu (<i>Institute of Microelectronics, Tsinghua University; Electronic engineering. Tsinghua University</i>)
P2-39	0740: SPICE Modeling and Simulation of High-Performance Wafer-Scale MoS2 Transistors
	Yuting Yao, Manxin Li, Tianxiang Wu, Hu Xu, Shunli Ma, Wenzhong Bao, Junyan Ren (<i>State Key Laboratory of ASIC and System, School of Microelectronics, Fudan University</i>)
P2-40	0741: Customizing CMOS/ReRAM Hybrid Hardware Architecture for Spiking CNN

f	Tianzhi Xue, Baicheng Liu, Wenhao Sun, Song Chen, Yi Kang, and Feng Wu (<i>School of Microelectronics, University of Science and Technology of China</i>)
P2-41	0745: A Low Complexity DDS Based On Optimized CORDIC Algorithm
	Shang Ma, Xuesi Wang, Yongjie Li, Kai Long, Bixin Zhu, Xin Lei (<i>National Key Laboratory of Science and Technology on Communication, University of Electronic Science and Technology of China; Sichuan Institute of Solid State Circuit, CETC</i>)
P2-42	0747: An FPGA based Parallel Implementation for Point Cloud Neural Network
	Xitao Zheng, Mingcheng Zhu, Yuan Xu, Yutong Li (<i>School of Information and Electronics Engineering, Shenzhen University; College of Big Data and Internet, Shenzhen Technology University</i>)
P2-43	0766: Research and Implementation of TPC Coding In High Bit Rate Telemetry System
	Lili Zhang, Wen Kuang (<i>Institute of Electronic Engineering China Academy of Engineering Physics</i>)
P2-44	0797: An Area-Efficient Multi-Rate Digital Decimator
	Qi Li, Yujun Shu, Yongzhen Chen and Jiangfeng Wu (<i>College of Electronic and Information Engineering, Tongji University</i>)

Friday

Friday, November 1, 8: 30 – 10: 00

Friday, November 1, 8: 30 – 10: 00

Grand Ball Room

Keynote Session K4

Hotel Hilton 3rd Floor

Session Chair : Yong Lian

- K4-1** **Neural Networks on Chip: From CMOS Accelerators to In-Memory-Computing**
(8: 30-9: 15)
Prof. Yu Wang, Tsinghua University, China
- K4-2** **Chip-Scale Wave-Matter Interactions: A New Frontier for RF-to-Light CMOS**
Sensing and Metrology Systems (9: 15-10: 00)
Prof. Ruonan Han, MIT, USA

Friday, November 1, 10: 15– 12: 15

Friday, November 1, 10: 15 – 12: 15	Xi'An + Dalian Room
Session A6 : Circuit for Medical & other Applications	Hotel Hilton 4 th Floor
Session Chair : Fan Ye	

	Title
A6-1	0792: A Short Review of CMOS Multi Electrode Arrays for Neural Tissue Interfacing with High Spatiotemporal Resolution (Invited Paper)
10: 15	Roland Thewes, Norman Dodel, and Günther Zeck (<i>Chair of Sensor and Actuator Systems, Faculty of EECS, TU Berlin, Berlin, Germany; Natural and Medical Sciences Institute at University Tübingen, Reutlingen, Germany</i>)
A6-2	0735: High Intensity Focused Ultrasound for Noninvasive Medical Applications (Invited Paper)
10: 42	Ming Zhang, Nicolas Llaser (<i>Microsystems - C2N, University of Paris-Saclay, Univ. Paris Sud</i>)
A6-3	0312: Wireless Sensor Brain Machine Interfaces for Closed-loop Neuroscience Studies (Invited Paper)
11: 09	Xilin Liu, Milin Zhang, Han Hao, Andrew G. Richardson, Timothy H. Lucas, and Jan Van der Spiegel (<i>Department of Electrical and Systems Engineering, Department of Neurosurgery, University of Pennsylvania, Philadelphia, USA; Department of Electronic Engineering, Tsinghua University, Beijing, China</i>)
A6-4	0751: Design of CMOS integrated circuits for radiation hardening and its application to space electronics (Invited Paper)
11: 36	Yann Deval, Hervé Lapuyade and François Rivet (<i>Univ. Bordeaux, Bordeaux INP, CNRS UMR5218, Laboratoire IMS, Talence, France</i>)
A6-5	0723: An ASIC for Discriminating Single Photon Detector Signal of High- Speed Quantum Key Distribution System
12: 03	Yulong Zhu, Futian Liang, Xinzhe Wang, Bo Feng, Chenxi Zhu, Ge Jin (<i>State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China; Department of Modern Physics, University of Science and Technology of China</i>)

Friday, November 1, 10: 15 – 12: 15	Wuhan + Nanjing Room
Session B6 : EDA Technology	Hotel Hilton 4 th Floor
Session Chair : Yibo Lin	

	Title
B6-1	0782: OpenMPL: An Open Source Layout Decomposer (Invited Paper)
10: 15	Wei Li, Yuzhe Ma, Qi Sun, Yibo Lin, Iris Hui-Ru Jiang, Bei Yu, David Z. Pan (<i>The</i>

	<i>Chinese University of Hong Kong; Peking University; National Taiwan University; University of Texas at Austin)</i>
B6-2	0777: Advanced Reliability-Aware Verification for Robust Circuit Design (Invited Paper)
10: 45	Joddy Wang and Frank Lee (<i>Analog and Mixed-Signal Simulation, Design Group. Synopsys Inc.</i>)
B6-3	0517: A Fast Reduction Method for Path Process Variations Without Time-Consuming Training
11: 15	Wenjie Fu, Yu Zheng, Leilei Jin, Ming Ling (<i>National ASIC System Engineering Technology Research Center, Southeast University</i>)
B6-4	0534: A Precise Block-Based Statistical Timing Analysis with MAX Approximation Using Multivariate Adaptive Regression Splines
11: 27	Leilei Jin, Wenjie Fu, Yu Zheng, Hao Yan (<i>Southeast University, Nanjing, P.R. China, National ASIC System Engineering Technology Research Center</i>)
B6-5	0635: An Effective Detailed Routing Algorithm Considering Advanced VLSI Technologies
11: 39	Peng Zou, Xiqiong Bai, Yingjie Wu, Lifeng Wu, and Jianli Chen (<i>College of Mathematics and Computer Science, Fuzhou University; Empyrean Software, Inc., Beijing</i>)
B6-6	0471: An Exponential Dynamic Weighted Fair Queuing Algorithm for Task Scheduling in Chip Verification Platform
11: 51	Jiafeng Liu, Zhiyin Lu, Xie Xie, Jian Wang, Jinmei Lai (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
B6-7	0706: Automatic Hardware Design Tool Based on Reusing Transformation
12:03	Chongzhou Fang, Zaichen Zhang, Xiaohu You, and Chuan Zhang (<i>Lab of Efficient Architectures for Digital-communication and Signal-processing (LEADS), National Mobile Communications Research Laboratory, Southeast University; Purple Mountain Laboratories, Nanjing, China</i>)

Friday, November 1, 10: 15 – 12: 15	Happiness Room
Session C6 : Power Management	Hotel Hilton 3 rd Floor
Session Chair : Chung Fai Au-Yeung	

	Title
C6-1	0515: Automatic Correction of Current Imbalance for Multi-Phase COT Ripple-Based Control DC-DC Converter
10: 15	Shogo Katayama, Jing Li, Yifei Sun, Tran Minh Tri, Yasunori Kobori, Anna Kuwana, Haruo Kobayashi (<i>Dept. of Electronics and Informatics Graduate school of Science</i>)

	<i>and Technology, Gunma University, Japan)</i>
C6-2	0538: Dual-Source Energy Cooperative Harvesting Circuit with Single Inductor
10: 30	Hanze Zheng, Yinshui Xia (<i>Faculty of Electrical Engineering and Computer Science, Ningbo University</i>)
C6-3	0392: EMI Noise Reduction and Output Ripple Cancellation for Full-Wave Type Soft-Switching Converter
10: 45	Yifei Sun, Minh Tri Tran, Yasunori Kobori, Anna Kuwana, Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University, Japan</i>)
C6-4	0387: Minimum Output Ripple and Fixed Operating Frequency Based on Modulation Injection for COT Ripple Control Converter
11: 00	Minh Tri Tran, Yifei Sun, Yasunori Kobori, Anna Kuwana, Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University, Japan</i>)
C6-5	0537: Multi-Phase Full/Half Wave Type Resonant Converters with Automatic Current Balance against Element Variation
11: 15	Chen-Hao Zhang, Yi-Fei Sun, Tran Minh Tri, Yasunori Kobori, Anna Kuwana, and Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University, Japan</i>)
C6-6	0348: Overshoot Cancelation Based on Balanced Charge-Discharge Time Condition for Buck Converter in Mobile Applications
11: 30	MinhTri Tran, Yifei Sun, Yasunori Kobori, Anna Kuwana, Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University, Japan</i>)
C6-7	0523: Pulse Coding Control Switching Converter with Adjustable Conversion Voltage Ratio Notch Frequency Generation in Noise Spectrum
11: 45	Yifei Sun, Minh Tri Tran, Yasunori Kobori, Anna Kuwana, Haruo Kobayashi (<i>Division of Electronics and Informatics, Faculty of Science and Technology, Gunma University</i>)
C6-8	0445: Performance optimization for LDO regulator based on the differential evolution
12: 00	Jintao Li, Yanhan Zeng, Hailong Wu, Ruguo Li, Jun Zhangy and Hong-zhou Tan (<i>School of Physics & Electronic Engineering, Guangzhou University; School of Information Engineering, Guangdong University of Technology</i>)

Friday, November 1, 10: 15 – 12: 15	Fortune Room
Session D6 : Advanced Process I	Hotel Hilton 3 rd Floor
Session Chair : Shengkai Wang	

	Title
D6-1	0771: Experimentally Obtaining the Top and Edge Contact Resistivities of

	Nb-Doped MoS2 Films Using the Transmission Line Measurement (Invited Paper, abstract only)
10:15	Chao-Hsin Chien (<i>Department of Electronics Engineering and Institute of Electronics, Chiao-Tung University, Hsinchu, Taiwan</i>)
D6-2	0778: Nano Sheet of Nitrided and Fluoro-Graphene on MoS2 Transistors for Memory Devices (Invited Paper, abstract only)
10: 45	Chao-Sung LAI (<i>Chang Gung University, 259 Wen-Hua 1st Rd., Kwei- Shan, Tao-Yuan, Taiwan</i>)
D6-3	0577: Oxygen-plasma-based digital etching for GaN/AlGaIn high electron mobility transistors (Invited Paper)
11: 15	Jingyi Wu, Yang Jiang, Zeyu Wan, Siqi Lei, Wei-Chih Cheng, Guangnan Zhou, Robert Sokolovskij, Qing Wang, Guangrui (Maggie) Xia, Hongyu Yu (<i>School of Microelectronics, Southern University of Science and Technology; Department of Electric and Electronics Engineering, Southern University of Science and Technology</i>)
D6-4	0796: Realization of Nanoscale Neuromorphic Memristor Array with Low Power Consumption (Invited Paper)
11: 45	Caidie Cheng, Teng Zhang, Chang Liu, Jiadi Zhu, liying Xu, Xiaoqin Yan, Yuchao Yang, Ru Huang (<i>Key Laboratory of Microelectronic Devices and Circuits (MOE), Department of Micro/nanoelectronics, Peking University; State Key Laboratory for Advanced Metals and Materials, School of Materials Science and Engineering, University of Science and Technology Beijing</i>)

Friday, November 1, 13: 30 – 15: 30

Friday, November 1, 13: 30 – 15: 30

Xi'An + Dalian Room

Session A7: Processor Technology

Hotel Hilton 4th Floor

Session Chair : Hongbin Sun

	Title
A7-1	0389: Latency Minimal Scheduling with Maximum Instruction Parallelism
13: 30	Zhenghua Gu, Wenqin Wan, Chang Wu (<i>State-Key Lab of ASIC and Systems, School of Microelectronics, Fudan University; Shanghai Fudan Microelectronics Group</i>)
A7-2	0377: Radiation Hardened Design of Pipeline and Register File in Processor
13: 45	Li-Yi Xiao, Yuan-Gang Wang, Zu-Qiang Zhang, Jia-Qiang Li, Jie Li (<i>Microelectronic Center, Harbin Institute of Technology</i>)
A7-3	0424: The Design and Implementation of High Speed Hybrid Radices Reconfigurable FFT Processor

14: 00	Qiao Yuan, Huajian Zhang, Yukun Song, Chongyang Li, Xueyi Liu, Zheng Yan (<i>Space Star Technology Limited Corporation, Beijing, China; Hefei University of Technology</i>)
A7-4	0710: Transparent Buffer Management: An Intra-cluster Task Scheduling Method Based on Dynamic Virtual Channel
14: 15	Guangqiu Lv, Wei Li, Tao Chen, Longmei Nan (<i>Institute of Information Science and Technology</i>)
A7-5	0441: Design and implementation of Serial ATA physical layer on FPGA
14: 30	Xie Xie, Qinghua Duan, Jiafeng Liu, Jian Wang, Jinmei Lai (<i>State Key laboratory of ASIC and System, Fudan University</i>)
A7-6	0695: High Parallel VLSI Architecture Design of BPC in JPEG2000
14: 45	Lintao Li, Jiangyi Shi, Zhixiong Di (<i>School of Microelectronics, XiDian University; The School of Information Science and Technology, Southwest Jiaotong University</i>)
A7-7	0527: An Asynchronous AER Circuits with Rotation Priority Tree Arbiter for Neuromorphic Hardware with Analog Neuron
15: 00	Jinsong Wei, Jilin Zhang, Xumeng Zhang, Zuheng Wu, Chunmeng Dou, Tuo Shi, Hong Chen, Qi Liu (<i>University of Science and Technology of China; Institute of Microelectronics Chinese of Academy of Sciences</i>)

Friday, November 1, 13: 30 – 15: 30	Wuhan + Nanjing Room
Session B7 : FPGA Technology	Hotel Hilton 4 th Floor
Session Chair : Jingmei Lai	

	Title
B7-1	0532: A Lightweight Slave-Module Interface Core to Implement IEEE 1149.5 MTM-Bus Based on FPGA
13: 30	Yalong Pang, Shuai Jiang, Luyuan Wang, Weiwei Liu and Jiyang Yu (<i>Beijing Institute of Spacecraft System Engineering</i>)
B7-2	0495: A Low-delay Configurable Register for FPGA
13: 45	Zhi-yin Lu, Jia-feng Liu, Yun-bing Pang, Zheng-jie Li, Yu-fan Zhang, Jin-mei Lai, Jian Wang (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
B7-3	0488: An FPGA-based log-structure Flash memory system for space exploration
14: 00	Huanlin Luo, Hai Ren, Tiantian Zhang, Jian Wang, Jinmei Lai (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
B7-4	0769: Balance of memory footprint and runtime for high-density routing in large-scale FPGA
14: 15	Wei Liu, Chengyu Hu, Peng Lu, Jinmei Lai (<i>State Key Laboratory of ASIC and System, Fudan University</i>)

B7-5	0487: Research on Area Modeling Methodology for FPGA Interconnect Circuits
14: 30	Yunbing Pang, Jiqing Xu, Zhiyin Lu, Zhengjie Li, Yufan Zhang, Jinmei Lai (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
B7-6	0770: Research on the impact of different benchmark circuits on the representative path in FPGAs
14: 45	Jiqing Xu, Zhengjie Li, Yunbing Pang, Jian Wang, Jinmei Lai (<i>State Key Laboratory of ASIC and System, Fudan University</i>)
B7-7	0677: A Novel High-speed FPGA-based True Random Number Generator Based on Chaotic Ring Oscillator
15: 00	Xinning Liu, Song Jia, Hanzun Zhang (<i>Institute of Microelectronics, Peking University; Key Laboratory of Microelectronic Devices and Circuits, Peking University</i>)

Friday, November 1, 13: 30 – 15: 30	Happiness Room
Session C7 : Electro-Optical & High Speed Circuit	Hotel Hilton 3 rd Floor
Session Chair : Yann Deval	

	Title
C7-1	0788: Design of high speed drivers for 56Gb/s PAM4 optical communications in CMOS (Invited Paper)
13: 30	Nan Qi and Nanjian Wu (<i>State Key Laboratory of Superlattices and Microstructures, Institute of Semiconductors, Chinese Academy of Sciences; Center of Material Science and Optoelectronics Engineering, University of Chinese Academy of Sciences</i>)
C7-2	0361: Design of Current-Assisted Photonic Demodulator (CAPD) for Time-of-Flight CMOS Image Sensor (Invited Paper)
14: 00	Cristine Jin Estrada, Chen Xu, and Mansun Chan (<i>Dept. of ECE, HKUST, Clear Water Bay, Hong Kong SAR, China; SmartSens Technology, San Jose, CA</i>)
C7-3	0542: An adjustable amplitude and pulse-width laser modulation driver with active feedback for QKD experiments
14: 30	Chenxi Zhu, Futian Liang, Bo Feng, Xinzhe Wang, Yulong Zhu, Chengzhi Peng (<i>School of Cyberspace Security, University of Science and Technology of China; Chinese Academy of Sciences (CAS) Center for Excellence and Synergetic Innovation Center in Quantum Information and Quantum Physics, University of Science and Technology of China</i>)
C7-4	0639: A 40Gb/s Low Power Transmitter with 2-tap FFE and 40:1 MUX in 28nm CMOS Technology
14: 42	Wenbin He, Fan Ye and Junyan Ren (<i>State Key Laboratory of ASIC and System Department of Microelectronics, Fudan University</i>)

C7-5	0628: Configurable Hybrid Output Driver for GPIO with Wide Supply Voltage Range of 1.05V-3.70V
14: 54	Siddharth Katare, Nagaveni Subramanya (<i>Sankalp Semiconductor Pvt Ltd,</i>)
C7-6	0494: An electro-optical full-subtractor using hybrid-integrated silicon- graphene waveguides
15: 06	Ruo-Lan Yu, Wei Liang, Jie Zhang, Yan Li, Wei-Wei Chen, Peng-Jun Wang (<i>Faculty of Electrical Engineering and Computer Science, Ningbo University; College of mathematics, physics and electronic information engineering, Wenzhou University</i>)
C7-7	0416: Design of the admittance detecting circuit for silicon waveguides using the capacitor-integration method
15: 18	Hong-Xiang Li, Wen-Hui Li, Wei-Wei Chen, Peng-Jun Wang (<i>Faculty of Electrical Engineering and Computer Science, Ningbo University; College of mathematics, physics and electronic information engineering, Wenzhou University</i>)

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Session D7 : Device Reliability

Session Chair : Francis Balestra

Fortune Room

Hotel Hilton 3rd Floor

	Title
D7-1	0567: An assessment of RTN-induced threshold voltage jitter (Invited Paper)
13: 30	Jian Fu Zhang, Azrif Manut, Rui Gao, Mehzaheen Mehedi, Zhigang Ji, Weidong Zhang, and John Marsland (<i>Department of Electronics and Electrical Engineering, Liverpool John Moores University</i>)
D7-2	0779: Reverse-Bias Stability and Reliability of Enhancement-mode GaN-based MIS-FET (Invited Paper)
14: 00	Mengyuan Hua, Song Yang, Jin Wei, Zheyang Zheng, Jiabei He, and Kevin J. Chen (<i>Department of Electrical and Electronic Engineering, The Southern University of Science and Technology; Department of Electronic and Computer Engineering, The HongKong University of Science and Technology</i>)
D7-3	0783: Self-heating Induced Variability and Reliability in Advanced Logic Devices and Circuits (Invited Paper)
14: 30	Xiaoyan Liu, Wangyong Chen, Linlin Cai, Gang Du and Xing Zhang (<i>Institute of Microelectronics, Peking University; Beijing Engineering Research Center of Active Matrix Display</i>)
D7-4	0697: Synergistic Effect of BTI and Process Variations on Impact and Monitoring of Combination Circuit
15: 00	Linzhe Li, Liyi Xiao, Jie Li, He Liu, Zhigang Mao (<i>Microelectronics Center, Harbin Institute of Technology</i>)

D7-5	0687: Optimization of High Reliability and Wide SOA 100 V LDMOS Transistor with Low Specific On-Resistance
15: 15	Anna Kuwana, Jun-ichi Matsuda and Haruo Kobayashi (<i>Division of Electronics and Informatics, Gunma University, Japan</i>)

Friday, November 1, 15: 45 – 17: 45

Friday, November 1, 15: 45 – 17: 45	Xi'An + Dalian Room
Session A8: System Design & Implementation	Hotel Hilton 4 th Floor
Session Chair : Yun Chen	

	Title
A8-1	0401: Improved Discrete Wavelet Analysis and Principal Component Analysis for EEG Signal Processing
15: 45	YiHsiang Chen, Xiaoxin Cui, Kanglin Xiao, Dunshan Yu (<i>Key Laboratory of Microelectronics Devices and Circuits, Institute of Microelectronics, Peking University</i>)
A8-2	0307: An Automatically Selective Signal Combining Algorithm and System for Low SNR ECG Signals
16: 00	Leiyou Wang, Donghui Wang (<i>Institute of Acoustics, Chinese Academy of Science; Key Laboratory of Information Technology for Autonomous Underwater Vehicles, Chinese Academy of Science</i>)
A8-3	0305: An efficient ASIC Implementation of QARMA Lightweight Algorithm
16: 15	Conghui Zhao, Yingjian Yan, Wei Li (<i>Department of Microelectronics, Zhengzhou Institute of Information Science and Technology, Zhengzhou</i>)
A8-4	0688: Area-Efficient Parallel Stochastic Computing with Shared Weighted Binary Generator
16: 30	Lun Zhang, Weikang Qian, Hai-Bao Chen (<i>Department of Micro and Nano Electronics, Shanghai Jiao Tong University; University of Michigan-Shanghai Jiao Tong University Joint Institute, Shanghai Jiao Tong University</i>)
A8-5	0717: Efficient Belief Propagation List Decoding of Polar Codes
16: 45	Yuqing Ren, Weihong Xu, Zaichen Zhang, Xiaohu You, and Chuan Zhang (<i>Lab of Efficient Architectures for Digital-communication and Signal-processing (LEADS), National Mobile Communications Research Laboratory, Southeast University; Purple Mountain Laboratories, Nanjing, China</i>)
A8-6	0722: Flexible and Adaptive Path Splitting of Simplified Successive Cancellation List Polar Decoding

17: 00	Houren Ji, Yifei Shen, Zaichen Zhang, Xiaohu You, and Chuan Zhang (<i>Lab of Efficient Architectures for Digital-communication and Signal-processing (LEADS), National Mobile Communications Research Laboratory, Southeast University; Purple Mountain Laboratories, Nanjing, China</i>)
A8-7	0729: A New Uplink Channel Estimation Architecture for Massive MIMO Systems with PDMA
17: 15	Zhenhao Ji, Yahui Ji, Bolei Wang, Feifei Gao, Huizheng Wang, Chuan Zhang (<i>Lab of Efficient Architectures for Digital-communication and Signal-processing (LEADS), National Mobile Communications Research Laboratory, Southeast University; Purple Mountain Laboratories, Nanjing, China</i>)
A8-8	0342: The Digital Front End with Dual-box Digital Pre-distortion in All-digital Quadrature Transmitter
17: 30	Yan Hu, Tao Wang, Zhiliang Hong (<i>State Key Laboratory of ASIC & System, Fudan University</i>)

Friday, November 1, 15: 45 – 17: 45 Session B8 : Chip Test & Reliability Session Chair : Ming Zhang	Wuhan + Nanjing Room Hotel Hilton 4 th Floor
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B8-1	0506: Multi-Thread Assembling for Fast FEM Power Delivery DC Integrity Analysis (Invited Paper)
15: 45	Ke Yang, Shaoyi Peng, Sheldon X.-D. Tan, Hai-Bao Chen (<i>Department of Micro/Nano-electronics, Shanghai Jiao Tong University; Department of Electrical and Computer Engineering, University of California, Riverside, USA</i>)
B8-2	0634: A Web-based Waveform Viewer for BR0101 Chip Testing Platform
16: 15	Xinyu He, Xie Xie, JinmeiLai, JianWang (<i>School of Microelectronics, Fudan University</i>)
B8-3	0463: An Accurate and Efficient Yield Analysis for SRAM dynamic metrics Using Differential Evolution Algorithm
16: 30	Liang Pang, Yifan Chai, Mengyun Yao, Yaqing Men, Xuexiang Wang, Longxing Shi (<i>School of Microelectronics, Southeast University; School of Electronic Science & Engineering, Southeast University</i>)
B8-4	0344: Evaluation of Null Methodfor Operational Amplifier Short-Time Testing
16: 45	Riho Aoki, Shogo Katayana, Yuto Sasaki, Kosuke Machida, Takayuki Nakatani , Jianlong Wang, Anna Kuwana, Kazumi Hatayama, Haruo Kobayashi, Keno Sato, Takashi Ishida, Toshiyuki Okamoto and Tamotsu Ichikawa (<i>Division of Electronics and Informatics, Gunma University, Japan; ROHM Semiconductor Co., Ltd., 2-4-8 Shin Yokohama, Kohoku-ku, Yokohama, Japan</i>)

B8-5	0654: Temperature Dependence of Bias Temperature Instability (BTI) in Long-term Measurement by BTI-sensitive and -insensitive Ring Oscillators Removing Environmental Fluctuation
17: 00	Takuya Asuke, Ryo Kishida, Jun Furuta, and Kazutoshi Kobayashi (<i>Department of Electronics, Graduate School of Science and Technology, Kyoto Institute of Technology, Japan; Department of Electrical Engineering, Faculty of Science and Technology, Tokyo University of Science, Japan</i>)
B8-6	0432: Adaptive Low-Rank Tensor Approximation for SRAM Yield Analysis using Bootstrap Resampling
17: 15	Xiao Shi, Hao Yan, Jiajia Zhang, Jinxin Wang, Longxing Shi, Lei He (<i>Electrical and Computer Engineering Dept., University of California, Los Angeles, CA, USA; State Key Lab of ASIC & System, Microelectronics Dept., Fudan University, China</i>)
B8-7	0474: A Single-Event Upset Evaluation Approach Using Ion-Induced Sensitive Area
17: 30	Ruiqiang Song, Jinjin Shao, Bin Liang, Yaqing Chi and Jianjun Chen (<i>College of Computer, National University of Defense Technology</i>)

Friday, November 1, 15: 45 – 17: 45	Happiness Room
Session C8: Clock Technology	Hotel Hilton 3 rd Floor
Session Chair : Mansun Chan	

	Title
C8-1	0380: Synthesizable Injection-Locked Phase-Locked Loop with Multiphase Interlocking Digitally Controlled Oscillator Arrays (Invited Paper)
15: 45	Yu-Cheng Su, Kang-Yu Chang, Yu-Tung Chin, Chia-Wen Chang and Shyh-Jye Jou (<i>Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Hsinchu, Taiwan</i>)
C8-2	0806: A CMOS Random Number Generator with Noise-Coupled Voltage-Controlled Oscillators (Invited Paper)
16: 09	Chung Fai Au-Yeung, Yiu Kei Li (<i>United Microelectronic Centres (Hong Kong) Limited</i>)
C8-3	0743: A Low-Power Comparator-Less Relaxation Oscillator
16: 33	Yufei Sun, Yanzhao Ma, Kai Cui, and Xiaoya Fan (<i>School of Software, Northwestern Polytechnical University; School of Microelectronics, Northwestern Polytechnical University</i>)
C8-4	0724: A Simple Steady Timing Resilient Sample Based on Delay Data Sense Detection
16: 45	Xuemei Fan, Rujin Wang, Qin Zeng, Hao Liu, ShengLi Lu (<i>National ASIC System</i>)

	<i>Engineering Technology Research Center, Southeast University)</i>
C8-5	0696: A wide range and high resolution two-step TDC for millimeter-wave band ADPLL
16: 57	Jieyang Li, Ting Yi, Zhiliang Hong (<i>State Key Lab. of ASIC and System, Dept. of Microelectronics, Fudan University</i>)
C8-6	0730: Output Voltage Ripple Reduction with Noise Spread Spectrum for Dual-Phase LLC Resonant Converter
17: 09	Shogo Katayama, Noriyuki Oiwa, Yasunori Kobori, Anna Kuwana, Haruo Kobayashi (<i>Division of Electronics and Informatics Graduate School of Science and Technology, Gunma University, Japan</i>)
C8-7	0715: A Class-F3 VCO with 104% Ultra-Wide Band Tuning Range and -125dBc/Hz Phase Noise
17: 21	Haoyang Zhou, Wei Li, Tao Wang, Jiao Ye, Chuanguo Wang (<i>School of Microelectronics, Fudan University</i>)
C8-8	0658: Design of Aging Detection Sensor Based on Voltage Comparison
17: 33	Haiming Zhang, Pengjun Wang, Yuejun Zhang, Yunfei Yu (<i>Faculty of Electrical Engineering and Computer Science, Ningbo University; State Key Laboratory of Cryptology, P. O. Box 5159, Beijing, China</i>)

Friday, November 1, 15: 45 – 17: 45	Fortune Room
Session D8 : Advanced Process II	Hotel Hilton 3 rd Floor
Session Chair : Jian Fu Zhang	

	Title
D8-1	0780: High performance optoelectronics based on CVD MoS₂ (Invited Paper)
15: 45	Qianlan Hu, Zhenfeng Zhang, Yanqing Wu (<i>Wuhan National High Magnetic Field Center and School of Optical and Electronic Information, Huazhong University of Science & Technology; Institute of Microelectronics and Key Laboratory of Microelectronic Devices and Circuits (MoE), Peking University</i>)
D8-2	0349: Rapid Growth of SiO₂ on SiC with Low Dit using High Pressure Microwave Oxygen Plasma (Invited Paper)
16: 15	Shengkai Wang, Jilong Hao, Nannan You, Yun Bai and Xinyu Liu (<i>Institute of Microelectronics of Chinese Academy of Sciences; University of Chinese Academy of Sciences</i>)
D8-3	0555: Solution Processed Metal Oxide in Emerging Electronic Devices (Invited Paper)
16: 45	Chun Zhao, CeZhou Zhao and TianShi Zhao (<i>Department of EEE, Xi'an</i>

	<i>Jiaotong-Liverpool University; Department of EEE, University of Liverpool, Liverpool L69 3GJ, UK)</i>
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ASICON 2019 Technical Sessions Overview

Date	Time	Xi'An + Dalian Room (A) (4 rd Floor)	Wuhan + Nanjing Room (B) (4 rd Floor)	Happiness Room (C) (3 th Floor)	Fortune Room (D) (3 th Floor)
OCT.29	9:00:12:15 14:00-17:15	Tutorial Session T1 & T2 Tutorial Session T3 & T4			
Oct.30	8: 30-9: 00	Opening (Grand Ball Room, 3 rd Fl.)			
	9: 00-10: 30	Keynote Session K1-1 & K1-2 (Grand Ball Room, 3 rd Fl.) Session Chair : Jan Van der Spiegel			
	10: 45-12: 15	Keynote Session K2-1 & K2-2 (Grand Ball Room, 3 rd Fl.) Session Chair : Rechard. M. M. Chen			
	13: 30-15: 30	Session A1 Digital Unit & Module Session Chair : Chua-Chin Wang	Session B1 Efficient AI Hardware Session Chair : Kyeong-Sik Min	Session C1 Security Technology Session Chair : Dongshen Liu	Session D1 Power Device Session Chair : Mengyuan Hua
	15: 45-17: 45	Session A2 Signal Processing Session Chair : Ngai Wong	Session B2 Computing-in/near-Memory I Session Chair : Minhao Yang	Session C2 ADC Circuit Session Chair : Yongzheng Chen	Session D2 Device Simulation & Integration I Session Chair : Toshiro Hiramoto
	17: 45-18: 45	IEEE CASS YP (Young Professionals) Session	Poster Session I Session Chair : Min Liu		
	19: 00-21: 00	Reception			
Oct.31	8: 30-10: 00	Keynote Session K3-1 & K3-2 (Grand Ball Room, 3 rd Fl.) Session Chair : Hidetoshi Onodera			
	10: 15-12: 15	Special Session A3 Efficent Digital Designs & Applications Session Chair : Chuan Zhang	Session B3 Computing-in/near-Memory II Session Chair : Tzu-Hsien Sang	Session C3 DAC & other Data Converter Module Session Chair : Tai-Cheng Lee	Session D3 Device Simulation & Integration II Session Chair : Pei-Wen Li
	13: 30-15: 30	Special Session A4 Smart Circuit and System I Session Chair : Sujuan Liu	Session B4 Memory & MEMS I Session Chair : Alan Seabaugh	Session C4 RF Circuit Session Chair : Kiat Seng Yeo	Session D4 Device Simulation & Integration III Session Chair : Kazuhiko Endo

Oct.31	15: 45-17: 45	Special Session A5 Smart Circuit and System II Session Chair : Xuexiang Wang	Session B5 Memory & MEMS II Session Chair : Jianguo Yang	Session C5 Wireless & Energy Harvesting Circuit Session Chair : Minoru Fujishima	Session D5 Novel Device Session Chair : Eddy Simoen
	17: 45-18: 45	Poster Session 2 Session Chair : Yi Zhao			
Nov. 1	8: 30-10: 00	Keynote Session K4-1 & K4-2 (Grand Ball Room, 3rd Fl.) Session Chair : Yong Lian			
	10: 15-12: 15	Session A6 Circuit for Medical & other Application Session Chair : Fan Ye	Session B6 EDA Technology Session Chair : Yibo Lin	Session C6 Power Management Session Chair : Chung Fai Au-Yeung	Session D6 Advanced Process I Session Chair : Shengkai Wang
	13: 30-15: 30	Session A7 Processor Technology Session Chair : Hongbin Sun	Session B7 FPGA Technology Session Chair : Jingmei Lai	Session C7 Electro-Optical & High Speed Circuit Session Chair : Yann Deval	Session D7 Device Reliability Session Chair : Francis Balestra
	15: 45-17: 45	Session A8 System Design & Implementation Session Chair : Yun Chen	Session B8 Chip Test & Reliability Session Chair : Ming Zhang	Session C8 Clock Technology Session Chair : Mansun Chan	Session D8 Advanced Process II Session Chair : Jian Fu Zhang
	19: 00-21: 00	Banquet			